Design and Implementation of a High Voltage Signal Generator for the Excitation of Electroluminescent Devices

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Master Thesis

Design and Implementation of a High Voltage Signal Generator for the Excitation of Electroluminescent Devices

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Herewith I declare, that I have made the presented paper myself and solely with the aid of the means permitted by the examination regulations of the Darmstadt University of Technology. The literature used is indicated in the bibliography. I have indicated literally or correspondingly assumed contents as such.

Darmstadt, November 2015

Peter Schuster

Abstract

This thesis discusses the design and implementation of a driver circuit for the excitation of electroluminescent devices. The system consists of a high voltage signal generator, dedicated power supplies for multiple supply voltages and a control block to adjust the parameters of the system via a connected computer. The designed system also allows the interconnection of multiple driver boards sharing a single control connection to a computer.

The following chapters contain a discussion of the design decisions and implementation details of this circuit and an explanation of the inner workings as well as exterior interfaces of the system. Measurements proving the performance of the assembled system as well as the stability of critical circuit blocks conclude the foregoing discussions. A final conclusion evaluates the findings gained from the design of this system and gives an outlook to possible further improvements and extensions.

Acronyms

ADC Analog-to-Digital Converter. 28, 29, 39, 42, 43

BJT Bipolar-Junction Transistor. 26

CRC Cyclic Redundancy Check. 61

DAC Digital-to-Analog Converter. 14, 18, 19, 22, 25, 39, 43, 64–67, 75

DMA Direct Memory Access. 67

EL Electroluminescence. 1–3, 5, 6, 9, 28, 76

ESL Equivalent Series Inductivity. 34

ESR Equivalent Series Resistance. 34

FET Field Effect Transistor. 7, 9

FFT Fast Fourier Transformation. 11

I^2C Inter-Integrated Circuit. 37, 39, 43

IC Integrated Circuit. 6, 8–10, 19, 25, 29–33, 35–37, 39, 40, 42–45, 47, 50, 54–58, 67, 72

LED Light Emitting Diode. 38, 43, 46, 47, 67, 68

MOSFFT Metal–Oxide–Semiconductor Field-Effect Transistor. 33, 34, 45, 46, 73

PCB Printed Circuit Board. 5, 44, 50–55, 58, 77

PWM Pulse With Modulation. 7, 30

RAM Random Access Memory. 39, 41, 46, 47, 61, 68, 71

SPI Serial Peripheral Interface. 23, 37–39, 42, 67

SWD Serial Wire Debug. 41, 42

TTL Transistor–transistor logic. 23

UART Universal Asynchronous Receiver Transmitter. 37–39, 43, 44, 46, 48, 58, 61, 68, 70, 71

USB Universal Serial Bus. 46, 47, 49, 57, 68–71

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1 Introduction

This chapter gives an overview of the general context of this project and the properties of electroluminescent (EL) devices. Although there are many other ways to efficiently generate light in electronic products, EL devices are still used in various applications requiring even light emission over a large, flat area, the possibility for very thin mechanical construction and high durability and lifetime. These are properties in which EL devices excel due to their simple construction with no active electronic parts. But the simplicity of EL devices demands high requirements for the driving circuitry involved in forming a system to bring EL devices to illumination. Designing a driver circuit for the excitation of EL devices for scientific use is the content of this master thesis.

1.1 The *ELSE* Project

This thesis is part of the project "*Elektrolumineszenz-Display in kapazitiver Sensorik (ELSE)*" which is set out to research and implement capacitive excitated, optoelectronic parts to support symbol recognition and operation with high efficiency and low waste arisings [1].

This technology is developed in corporation with other research institutes and companies. As a first application it should be used to illuminate push buttons as seen in public transport for better recognition at night (see figure 1.1).

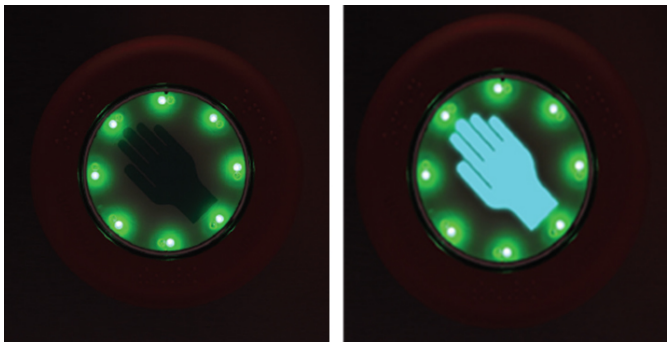

Figure 1.1.: State of the art: A button in dark environment (left: hand symbol not recognizable, right: project aim, self-illuminated symbol). [1]

The designed circuit is to be used to specify optimal operating parameters for the excitation of the produced EL devices in endurance tests by print technology engineers. Therefore, it has to be simple in use, stable and allow for a wide range of operating parameters.

The findings obtained in these endurance tests under varying parameters are then to be used for the design of a highly integrated system supplying the excitation signal for the optimal operating point of the EL devices both in regards of illumination and endurance. This further step is done at the *Integrated Electronic Systems Lab* at the *TU Darmstadt* and is not part of this thesis.

1.2 Electroluminescent Devices

Electroluminescence (EL) describes the non-thermal generation of light by frequently changing high voltages applied to a solid dielectric foil. The structure of EL lamps is shown in figure 1.2. The transparent electrode at the top layer is usually made of ~0.3 mm polyester or polycarbonate materials and equipped with a 0.5 μm coating of conducting indium tin oxide (ITO) [2, p. 2]. The two electrodes are electrically separated by the dielectric layer on top of the back electrode and form a leaky capacitor. Charging this capacitor with alternating polarity applies an electric field to the phosphor layer in the middle. Due to the

non-perfect isolation between the electrodes, electrons move along the lines of the electric field through the phosphor layer. Applying high voltages to the electrodes leads to a high energy level of electrons moving through the insulation/phosphor layer. When the energy level of the electrons is high enough to "excite luminescent centers through the impact excitation mechanism" [2, p. 2], light emission occurs in the phosphor layer. It can be observed that the amount of emitted light and color (combination of wavelengths) depends on the amount of applied voltage and switching frequency of the signal at the electrodes [2, p. 2].

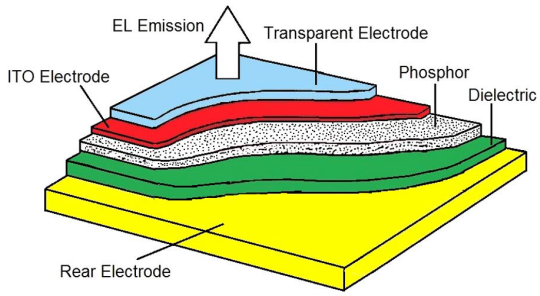

Figure 1.2.: AC powder EL lamp structure [2, fig. 1, p. 2].

To model the electric behavior of EL devices, an equivalent circuit has to be specified inheriting the behavior at intended operating conditions. This can be accomplished by observing the frequency response of the EL devices in a test setup. Doing this leads to an equivalent circuit for EL devices as shown in figure 1.3. The circuit consists of a capacitor with one resistor in series and one resistor in parallel. In practice EL devices consist of a lot of this circuits in parallel distributed over the whole surface area of the device.

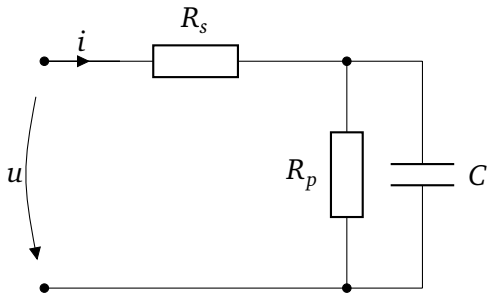

Figure 1.3.: Electroluminescent device model.

To specify the expected load for the to be designed system, measurements on prototypes of the produced EL devices were conducted prior to this thesis project [3]. Table 1.1 shows the minimum and maximum boundaries of the circuit components measured at tested EL devices.

Table 1.1.: EL device specification measurements.

	min	**max**
C	2.84 nF	5.28 nF
R_S	479.1 Ω	1.40 kΩ
R_P	12.69 MΩ	25.55 MΩ

2 Project Overview

Design and implementation of a high-voltage signal generator for the excitation of EL devices is the main part of this thesis, but the design of any device requires well understood requirements and an evaluation of possible architectures and approaches to reach the design goal. These are the topics of the following overview chapter.

2.1 Preceding Work

Research on the topic of EL devices and suitable driver circuits was already conducted prior to this thesis at the *Integrated Electronic Systems Lab* at the *TU Darmstadt*. The findings and concluded requirements for tools to be used in a lab environment lead to an implementation using an *H bridge* based driver circuit built in a bachelor thesis [4] and optimized in a semester project [5]. The resulting implementations were used to test the excitation of EL devices in the lab, but do not cover the required range for the relevant operating parameters specified for this project and lack stability for usage in long-time endurance tests.

Therefore, the goal to design a new system fulfilling the requirements in the context of the *ELSE* project was set. However, the knowledge gained in the design process involved in building the previous implementations and findings concerning the implementation of a high-voltage driver influenced the design of the high-voltage signal generator discussed in this thesis.

2.2 Requirements

The key requirements for the design of the high-voltage signal generator were given in the project description and can generally be inferred from the planned application for testing EL devices with a wide range of working conditions. Table 2.1 shows an overview of these requirements which are discussed in the remainder of this section.

Table 2.1.: Requirements for the high-voltage signal generator.

Input Voltage	24 – 70 V (DC)
Output Voltage	0 – 400 V_{pp}
Frequency	10 – 5000 Hz
Signal	sine and pulse
Load	up to 10 nF
Cost	150-200 Euro

The device has to work with an input voltage between 24 and 70 V DC. The output voltage has to be adjustable between 0 and 400 V peak-to-peak, whereas the lower voltage range is not of very high importance, but it needs to be possible to switch the output of the device off. The device has to work with an operating frequency range from 10 to 5000 Hz and has to be able to generate arbitrary waveforms. At a minimum sine and pulse (square) signal forms need to be supported.

The device needs to be able to drive a load capacitance of up to 10 nF over the complete operating frequency range. This means that the connected load needs to be completely charged (discharged) in a time period half the signal period. The general equation for capacitor load processes is of exponential

form and therefore does not have a distinct time point indicating the end of charge (discharge) processes. Equation 2.1 shows the correlation between the load properties (capacitance C and series resistance R), the voltage at the output terminals of the device (V_0) and the resulting voltage over time ($V(t)$):

$$V(t) = V_0 \cdot \left(1 - e^{-\frac{t}{RC}}\right) \tag{2.1}$$

Using this equation, it can be inferred that a capacitor charge of 99 % is reached after 5 RC with RC being the time constant of the system:

$$0.99 \cdot V_0 = V_0 \cdot \left(1 - e^{-\frac{t}{RC}}\right) \tag{2.2}$$

$$1 - 0.99 = e^{-\frac{t}{RC}} \tag{2.3}$$

$$\ln(1 - 0.99) = -\frac{t}{RC} \tag{2.4}$$

$$t = -\ln(1 - 0.99) \cdot RC \approx 5 \cdot RC \tag{2.5}$$

The maximum required switching frequency is 5 kHz, which leads to a minimum charge (discharge) time of $t_{\mathrm{c,min}} = 0.1$ ms. Combined with the calculated time constant of $5 \cdot RC$ and the required maximum capacitance of 10 nF this yields a maximum series resistance of

$$R_{\mathrm{max}} = \frac{0.02\ \mathrm{ms}}{10\ \mathrm{nF}} = 2\ \mathrm{k\Omega}. \tag{2.6}$$

The measured sample devices (see table 1.1) have a series resistance below this calculated maximum value. It is therefore possible to drive the devices and perform full charge and discharge of the capacitances.

Ohm's law yields the maximum current to be supplied for a full voltage swing from −200 V to +200 V to

$$I_0 = \frac{V_0}{R_{\mathrm{max}}} = \frac{400\ \mathrm{V}}{2\ \mathrm{k\Omega}} = 200\ \mathrm{mA}. \tag{2.7}$$

Therefore, the designed device needs to be able to supply a maximum current of 200 mA being the initial current for a 2 kΩ series resistance at the full output voltage swing of ±200 V. Lower series resistances than the calculated maximum resistance lead to higher peak currents, therefore an additional safety margin is incorporated in the deducted requirements for the current drive capabilities of the device leading to a design goal of 300 mA instantaneous current drive capability.

The average current to be supplied by the device at maximum load conditions can be calculated to

$$I = \frac{Q}{t} = \frac{V_0 \cdot C}{t_{\mathrm{c,min}}} = \frac{400\ \mathrm{V} \cdot 10\ \mathrm{nF}}{0.1\ \mathrm{ms}} = 40\ \mathrm{mA}. \tag{2.8}$$

Beside these electrophysical requirements for the to be designed device, two additional administrative requirements where given upon project start: The designed device is to be manufactured with a quantity of 45 to 50 devices. Therefore the maximum cost per device should not exceed 150 to 200 euro. The second non-technical requirement is that control of the designed devices should be possible through a connection to a personal computer using standard software (*Matlab*, *LabView*, etc.). Furthermore it should be possible to link multiple boards with one single/shared connection to a computer.

2.3 Design Overview

From the presented requirements a first general key characteristic of the overall system can be deducted: The demanded ability to control multiple driver circuits through one connection to a computer, suggests a multi-board design consisting of a controller board and separate driver boards to generate the output signals for the EL devices. Separating the functionality to communicate with external systems (computer) into a second, decoupled board allows to focus on the implementation of technical requirements on the driver board while placing advanced communication functionality and arbitration of multiple driver boards on a second system.

The connection of multiple driver boards to a single controller board could be accomplished in a series configuration, by chaining the driver boards, or in a parallel configuration through multiple connectors on the controller board. Both solutions have advantages and disadvantages: In a series configuration cables, connectors, and connecting traces on the driver board PCB need to be able to carry the current for the maximum number of devices in series. Additionally, the communication protocol that is to be implemented, needs to be able to address individual devices on the same bus and provide mechanisms to prevent or detect collisions. In a parallel configuration additional connectors and transceiver modules need to be fitted on the controller board and the system needs to implement multiple parallel communication channels.

To support a sufficient amount of devices per controller board while still utilizing readily available, inexpensive cables and connectors, it was decided to build a design featuring a combination of both approaches resulting in a four channel design supporting at least four devices (driver boards) per channel. This leads to a total of 16 supported driver boards per controller.

Figure 2.1 shows this design with four channels ("A" to "D") and four connected driver boards per channel. Each of the driver boards can be connected to a single load (EL device).

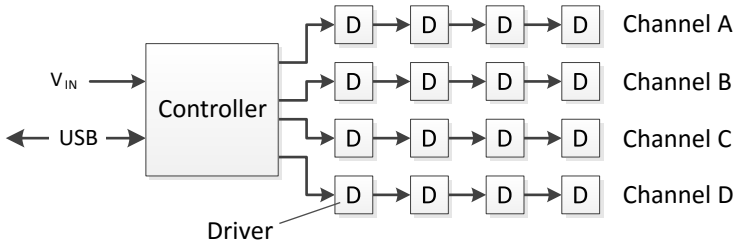

Figure 2.1.: 4x4 channel design of the high-voltage signal generator system.

2.4 Driver Designs

The design of a controller board acting as a communication hub between a connected computer and the driver boards is a standard problem which can be solved by a solely digital system consisting of one of

many available microcontrollers and some supporting circuitry for driving the distinct communication buses.

The design of the driver board is more challenging, containing multiple analog sub circuits and high-voltage components. The following sections discuss a variety of possible approaches for driver designs, fulfilling the specified requirements to drive EL devices. The sections about distinct designs will give an overview over each considered design and elaborate strength, weaknesses and blockers.

The simplest solution is to use readily available integrated EL driver circuits. There are a number of these ICs available, but all have a very limited range for variation in operating parameters. Most of the available solutions only allow a variation of the output frequency or voltage.

Table 2.2 shows an overview containing most of the readily available commercial ICs.

Table 2.2.: Specifications of commercially available driver ICs.

Manufacturer	**Part**	$V_{\mathbf{max}}$ / **V**	$V_{\mathbf{min}}$ / **V**	$f_{\mathbf{max}}$ / **Hz**	$f_{\mathbf{min}}$ / **Hz**
Microchip	HV816	360	n/a	1000	100
Microchip	HV860	220	n/a	500	150
Maxim-IC	MAX14514	300	n/a	250	250
Durel	D305A	400	n/a	525	425
Microchip	HV509	200	50	15625	0
Micrel	MIC4830	180	n/a	1000	60

None of these solution can be used to cover the required range of operating parameters. Using a solution incorporating one of these commercially available integrated driver circuits is therefore not an option for this project.

Solutions compiled from distinct components require three circuit blocks at minimum. A power supply block is required to provide the required voltages for a second circuit block generating the output signal. Both circuits need some form of control implemented in a third circuit block. This system is shown in figure 2.2 and will act as a base model for all following evaluations of possible approaches.

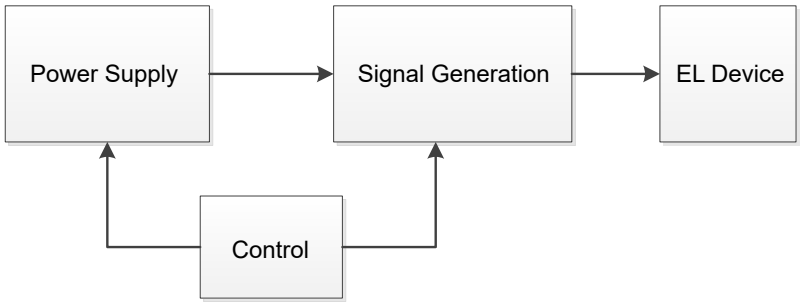

Figure 2.2.: Basic system architecture.

2.4.1 Power Supply

A driver board compiled from distinct components needs to include a power supply circuit to generate a high voltage supply voltage from the specified input voltage ranging between 24 and 70 V DC.

A common DC-DC converter solution with high efficiency is the class of switch-mode power supplies. Figure 2.3 show the basic circuit of a switch-mode power supply in step-up configuration:

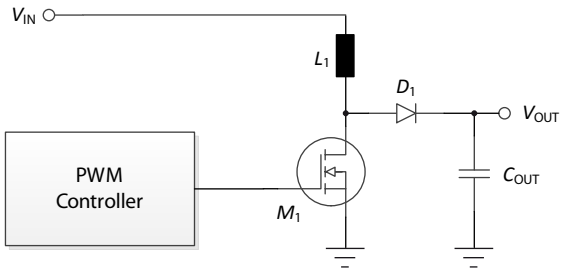

Figure 2.3.: DC-DC converter in step-up configuration.

A Pulse With Modulation (PWM) controller switches an N-MOS Field Effect Transistor (FET) (M_1) on and off to control the duty cycle of the inductor L_1. The output voltage is a function of input voltage and duty cycle of the switch/inductor and shown in equation 2.9:

$$V_{\text{out}} = V_{\text{in}} \cdot \frac{t_{\text{on}} + t_{\text{off}}}{t_{\text{on}}} \tag{2.9}$$

The duty cycle can be regulated using a feedback loop from the output voltage to an error amplifier. The error amplifier compares the feedback voltage (through voltage divider R_1-R_2) to a reference voltage and adjusts the duty cycle accordingly. The reference voltage can be obtained using a band-gap voltage reference.

Figure 2.4 shows the described feedback circuit:

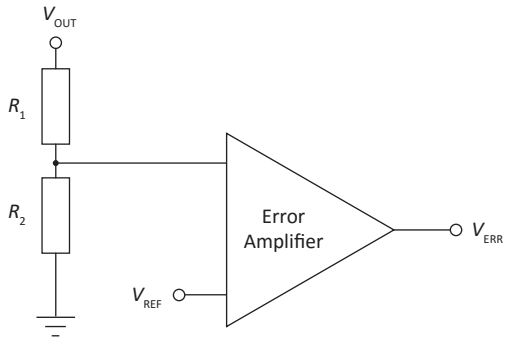

Figure 2.4.: Feedback loop to the error amplifier inside the PWM controller.

A power supply with adjustable output voltage can be implemented by replacing one of the resistors in the feedback path with an adjustable potentiometer. Adding a third, fixed resistor to the voltage divider limits the possible output voltage range and increases the linearity of the system controlled through the adjustable potentiometer.

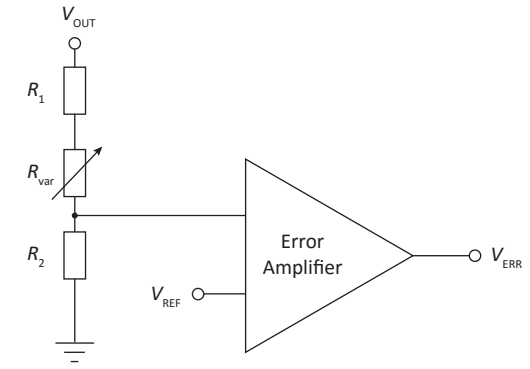

Figure 2.5.: Feedback loop to the error amplifier inside the PWM controller with an adjustable potentiometer.

Most integrated switch-mode power supply control circuits incorporate the shown error amplifier and might also contain a current sensing block, to regulate the output voltage in respect to a maximum output current.

A power supply designed, following the described principal of switch-mode power supplies, is used as a basic building block for the final system. The following sections discuss options for generating output signals with the required characteristics utilizing this power supply circuitry.

2.4.2 H Bridge

A standard design for generating alternating voltage/current (AC) signals from DC input voltages are so called H bridges, being one form of a power inverter circuit. They are also implemented in commercially available integrated circuit driver solutions which can be deducted from typical characteristics of H bridge generated AC signals being visible in the output signal generated by these ICs. An H bridge consists of four individually controlled switches connecting a load at the output terminals of the system to a positive supply voltage (V_{in}) as well as the negative supply voltage rail (i.e. ground). Figure 2.6 shows a schematic representation of the described H bridge circuit:

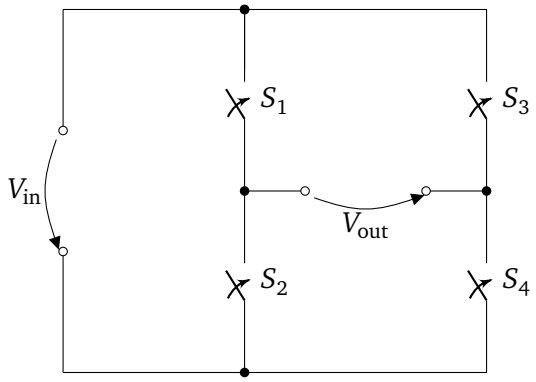

Figure 2.6.: H bridge circuit.

The H bridge works as inverter circuit transforming a DC input voltage to an alternating voltage at the output by switching the diagonal opposing switches (S_1 and S_4, as well as S_2 and S_3) synchronously. This

results in the output V_{out} of the system alternating between $+V_{in}$ and $-V_{in}$. An input voltage of 200 V yields therefore an output voltage of 400 V_{pp}.

The switches can be implemented by P-MOS (high side, S_1 and S_3) and N-MOS (low side, S_2 and S_4) FETs. The addition of a microcontroller for generating the control signals for the switches gives a simple solution for an H bridge based circuit driving EL devices:

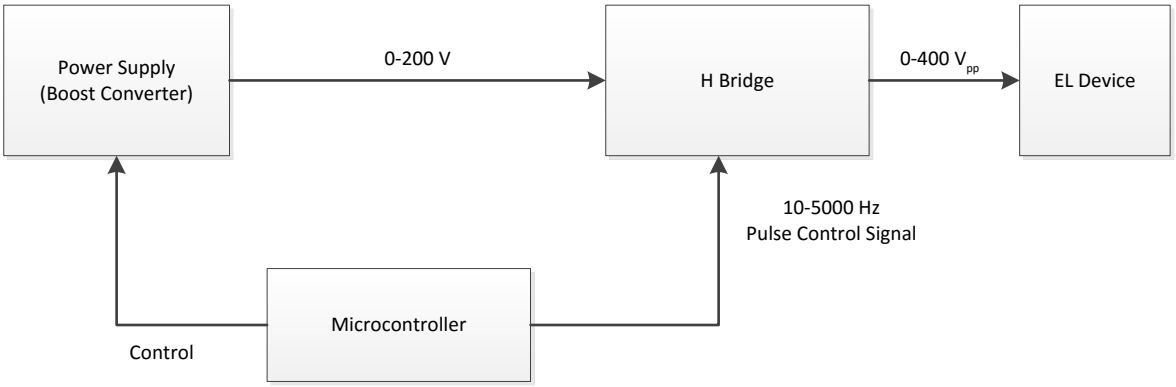

Figure 2.7.: H bridge based driver design.

The output voltage of the system is twice the voltage supplied by a power supply circuit build as a switching regulator. Therefore, the output voltage of this circuit can be controlled using a digital potentiometer in the feedback path of the error amplifier of the switch-mode controller IC, as described in section 2.4.1 (figure 2.5). The resistor values for this feedback network can be calculated from the maximum output voltage (200 V), the maximum voltage at the pins of the digital potentiometer and the minimum feedback voltage (V_{ref}).

The described system build around an H bridge inverter circuit can generate rectangular waveforms to drive EL devices, but requires additional solutions to generate signals with other, advanced waveforms. The following sub sections discuss three solutions to extend the described system for generation of advanced waveforms.

Signal Shaping - 1. Approach: Using an Adjustable Power Supply

One solution to achieve non-rectangular output signals would be to adjust the supply voltage generated by the power supply block to follow the required output signal form. To determine the practicability of this approach, a solution for generating a 400 V_{pp} sine wave at 5 kHz as shown in figure 2.8 is investigated.

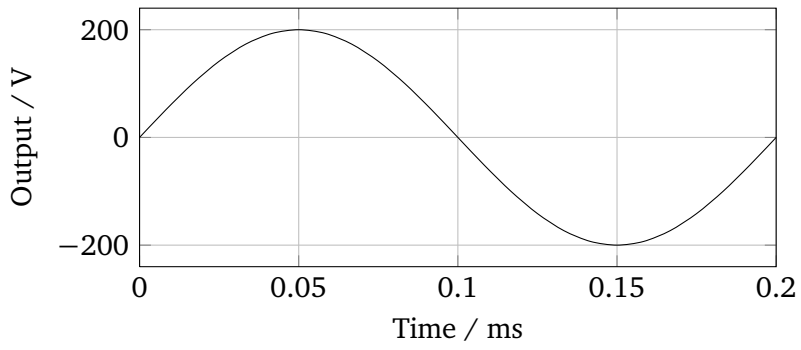

Figure 2.8.: 400 V_{pp} sine wave at 5 kHz.

A 400 V_{pp} sine wave output signal at 5 kHz requires a maximum supply voltage of 200 V (DC) and a switching frequency for the H bridge of 10 kHz. The signal fed into the H bridge needs to follow the positive half of the sine wave with an amplitude of 200 V and a frequency of 10 kHz.

To achieve this, the output voltage of the power supply needs to be adjusted to vary between 0 and 200 V with a frequency of 10 kHz. Furthermore, additional sampling points are required to form the sine wave, which in turn requires a control frequency with a multitude of the desired output frequency.

Existing digital potentiometer ICs can be operated with the required frequency (e.g. *Analog Devices*, AD5293: 50 MHz [6]) to set an output voltage following an arbitrary waveform, but the solution requires the switching regulator circuit to be stable and provide the required output voltage in a very short period of time. A look into the datasheet of the *LM3481*, a common boost controller IC by *Texas Instruments*, shows that the switching regulator IC needs about 20 ms to provide a stable 12 V output from a 5 V input (see figure 2.9). Neglecting the initial *slow start delay*, it still requires 8 ms to go from 5 V to 12 V at the output.

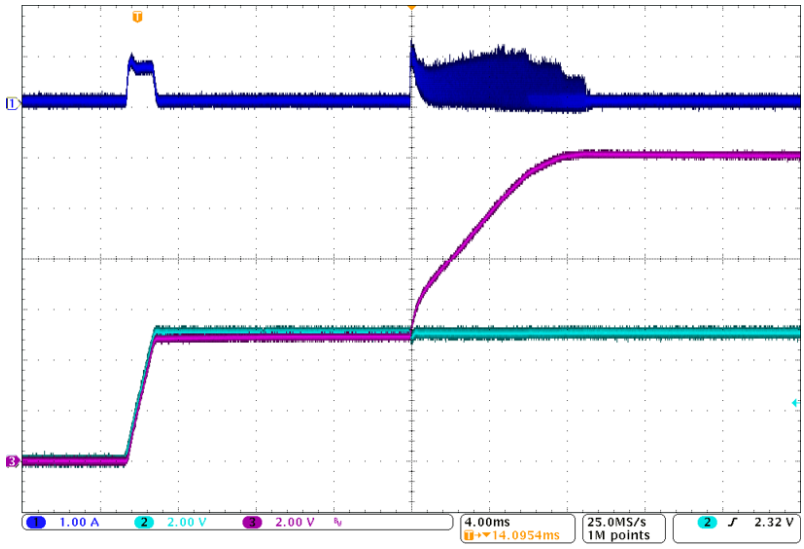

Figure 2.9.: Start-up pattern for a 5 V_{in}, 12 V_{out} boost converter using LM3481 boost evaluation module [7, p. 25].

The described application generating the positive half of a sine wave with 200 V amplitude requires a boost factor of up to 8 times the input voltage. Performed simulations at these operating conditions using manufacturer provided *SPICE* simulation models for switching regulator ICs showed, that using these standard, available ICs, it is not possible to get stable output voltages in less than 20 to 40 ms. This is rooted in their characteristic of providing a very stable output at a fixed voltage, which is opposing to the desired behavior in context of the planned application.

Designing a system implementing the given requirements is therefore not possible using the described approach.

Signal Shaping - 2. Approach: Filtering the Output Signal

A second possible solution to generate non rectangular (sine) signals using an *H bridge* based inverter circuit is to apply a low-pass filter to the output of the H bridge, filtering the unwanted frequencies of the

signal. This low-pass filter has to be switchable (on/off) and needs to have an adjustable cut-off frequency. It also needs to be suitable for an operating voltage of up to 400 V_{pp}.

Figure 2.10 shows a Fast Fourier Transformation (FFT) of a rectangular signal with a frequency of 50 Hz as it could be measured at the output of an H bridge circuit operated with respective parameters.

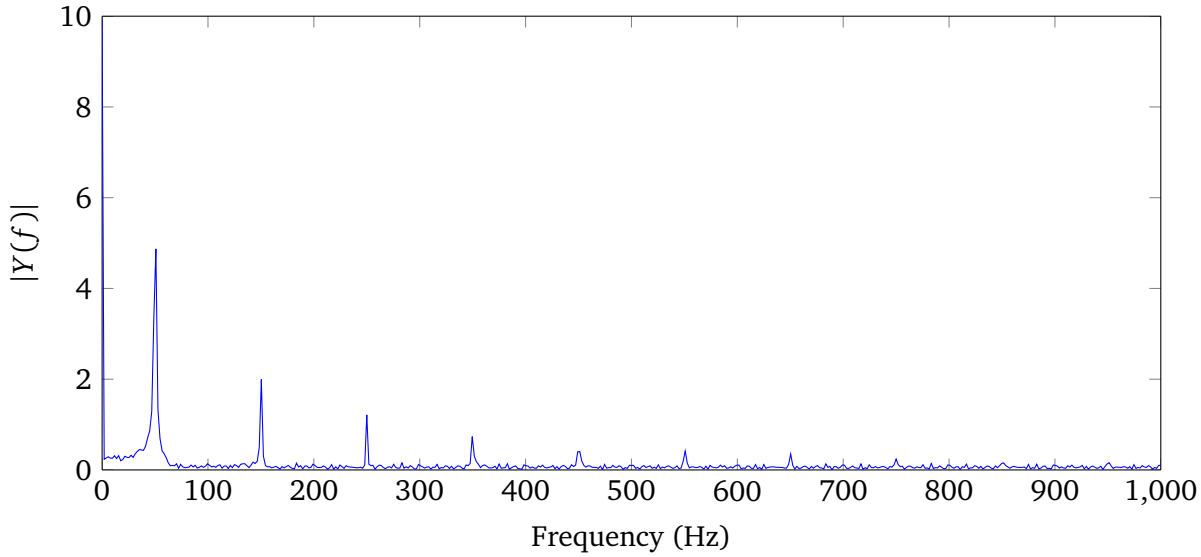

Figure 2.10.: FFT of a 50 Hz rectangular signal $y(t)$ with an amplitude of 10.

The plot shows that the frequency spectrum contains spikes at odd-numbered multitudes of the base frequency ($f_n = (2n+1) \cdot f_0$). To obtain a sinusoidal signal from an rectangular signal at the base frequency, the corner frequency of the low pass filter has to be set to about twice the base frequency, but has to be less than three times the base frequency. The required output frequency range from 10 to 5000 Hz requires therefore a low-pass filter with adjustable corner frequency in the range from 20 to 10000 Hz. The quality in terms of pureness of the sinusoidal output signal depends on the slope of the low-pass filter (Q factor).

Figure 2.11 shows a passive (a) and an active (b) first-order low-pass filter with a slope of -20 dB per decade [8, p. 578].

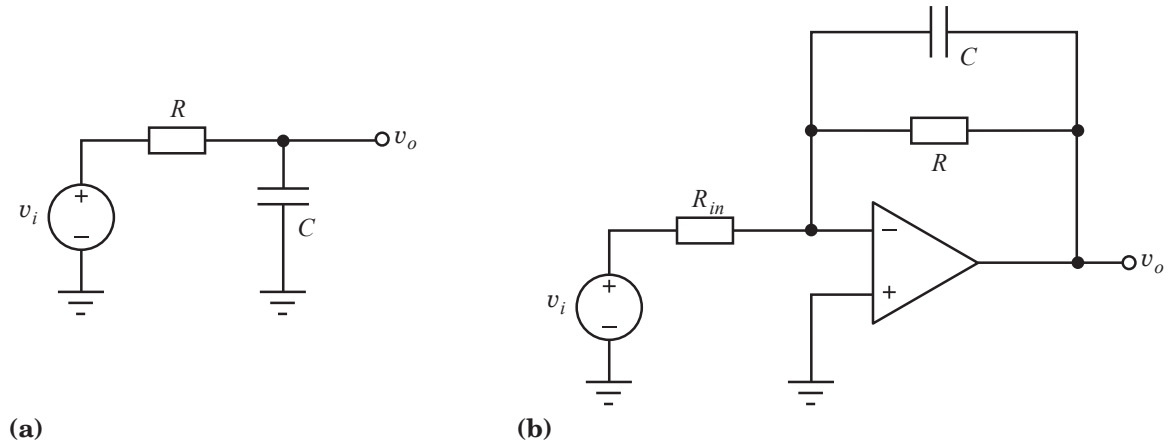

Figure 2.11.: Low pass filter: (a) passive and (b) active.

The corner (cut-off) frequency f_c is calculated for both designs according to equation 2.10 [8, p. 578]:

$$f_c = \frac{1}{2\pi RC} \tag{2.10}$$

Active low-pass filters have an operational amplifier in the main signal path. The design requirement for high output voltages implies that these operational amplifiers need to withstand voltages of up to 400 V_{pp}. Operational amplifiers with this characteristic are rarely available and highly priced[1]. Therefore, usage of these components is not in line with the specified budget and active low-pass filters with the presented circuit design can not be incorporated in a to be designed solution.

Any digitally adjustable resistor or capacitor is sensitive to high voltages, resulting in very high component prices or no commercially available solutions at all for the required 400 V_{pp} output voltage. Therefore, another approach circumventing the requirement of active adjustable filter components is to use a reverse quantization design with discrete, switchable capacitor components. Such a design is shown in figure 2.12:

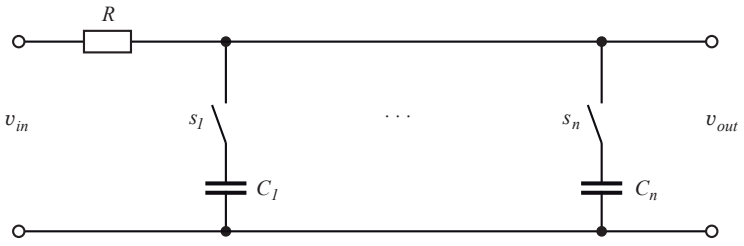

Figure 2.12.: Capacitor array.

Using the general equation for calculating the cut-off frequency (equation 2.10), the RC constant can be calculated for the minimum and maximum frequency to $RC_{20} = 7{,}957\ \mu\text{F}\,\Omega$ and $RC_{10\text{k}} = 15.92\ \mu\text{F}\,\Omega$.

A linear quantization of this capacitance range can be obtained from equation 2.11:

$$C_i = \frac{C_{\max}}{2^{n-i+1}} \quad i = 1,\ldots,n \tag{2.11}$$

The number of quantization steps required to cover the frequency range is a function of the minimal and maximal RC constant values and can be calculated to

$$n = \lceil \log_2 \left(\frac{RC_{\max}}{RC_{\min}} \right) \rceil = \lceil \log_2 (500) \rceil = 9. \tag{2.12}$$

For a resistance R of 10 Ω the highest capacitance C_9 has to be 397.85 μF. Capacitors in this range are predominantly implemented as polarized electrolytic capacitors. The output of the H bridge swings from

[1] APEX PA85 at Digikey (11/2015): 131.22 euro at 50 pcs. - http://www.digikey.de/product-detail/de/PA95/598-1335-ND/1761959

−200 V to +200 V, but a polarized capacitor does not withstand an alternating polarization across its connectors.

An alternative design to incorporate this technological limitation is shown in figure 2.13. It features a separate low-pass filter for both output connections of the H bridge (v_{in} terminals).

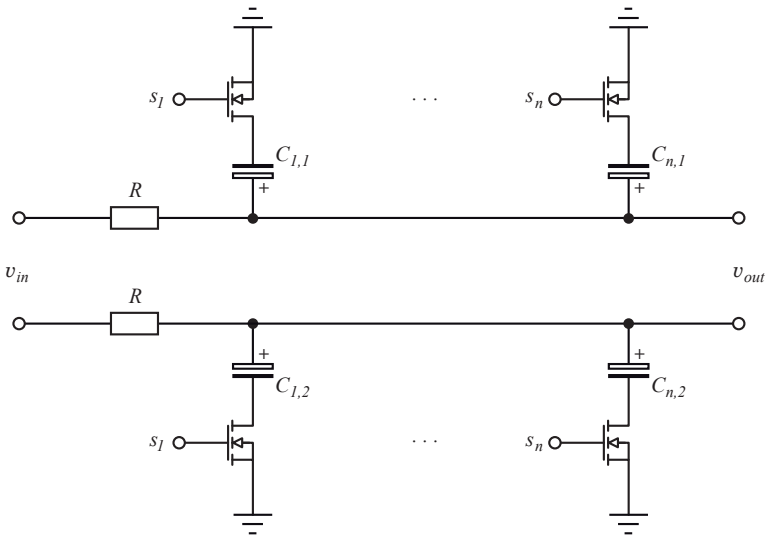

Figure 2.13.: Mirrored capacitor array.

This filter design provides a possibility to dynamically control the filter value by enabling or disabling capacitors between the output voltage rails and ground. A drawback of this solution is that a non-trivial part of the generated output signal is dissipated by continuously charging and discharging the capacitors forming the filter network. The power dissipation through this continuous charge and discharge activity of the low-pass filter is a function of the output voltage and the series resistances used in the filter network as shown in equation 2.13. The value of enabled capacitors in the filter network is a function of the frequency and therefore canceled out.

$$P = VI = \frac{VQ}{t} = CV^2 f = \frac{V^2}{2\pi R} \tag{2.13}$$

Maximum power dissipation occurs at maximum output voltage ($V = +200$ V) and can be calculated to $P_{\text{diss,max}} = 637$ W per output rail. This is a multitude of an acceptable power consumption for a small electronic device driving a capacitive load of 10 nF and therefore not a suitable solution.

Power dissipation and the required size of capacitors could be optimized by increasing the series resistance R, but the dissipation would still be large compared to the power required at the output of the device.

Signal Shaping - 3. Approach: Closed-loop Transistor Control

Another viable solution is to control the *H bridge* switching transistors like an amplifier stage and regulate the voltage by driving the transistors in the linear region.

This solution requires a closed-loop, self-regulating and adjustable control circuit which has great similarities with an operational amplifier, but also higher losses due to having an amplifier consisting of a single stage to provide the output voltage as well as the required current with transistors not operated in the saturation region.

Therefore, this approach is not pursued any further. The design of an high-voltage operational amplifier is discussed in section 2.4.4.

2.4.3 Output Transformer

Operational amplifiers for the required output voltage range of 400 V_{pp} are not in line with the project budget (see section 2.4.2). Furthermore, if operational amplifiers suitable for this voltage range are available, they can also be used for generating the desired waveforms without the need for an H bridge based inverter design. One approach to solve the trade-off between a technological viable solution and the requirement to meet a given budget for the project is to use operational amplifiers with a voltage rating as high as possible, while still being in line with the budget and bridge the remaining gap to the required maximum output voltage with a transformer connected to the operational amplifier stage.

Figure 2.14 shows an overview of the required components to build a design following the described approach:

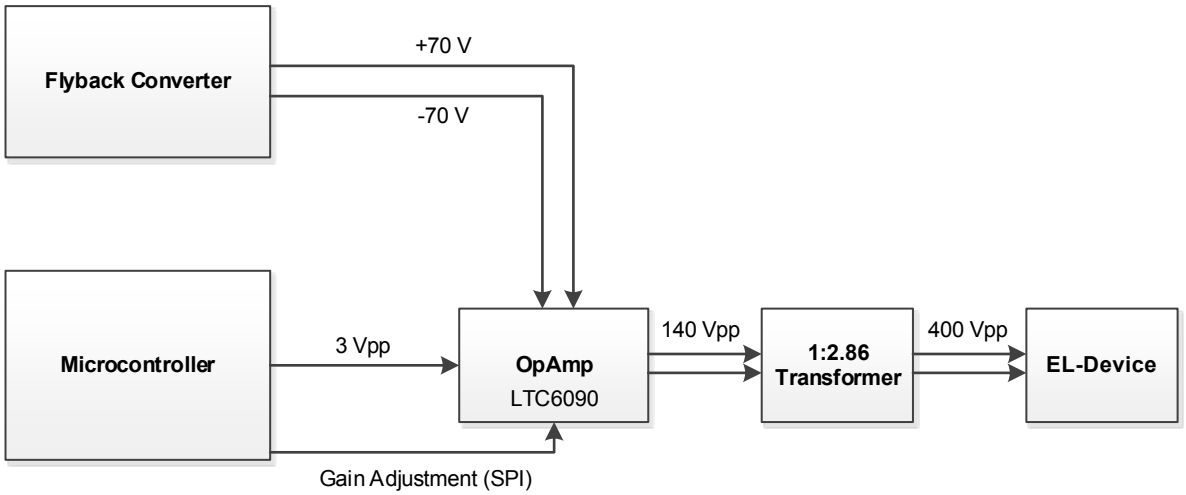

Figure 2.14.: Design featuring an output transformer.

The operational amplifier `LTC6090` by *Linear Technology* is build for a supply voltage of up to 140 V and in lower quantities still at a reasonable price point. With an output transformer ratio of 1:2.86 the 140 V_{pp} output of the operational amplifier can be transformed to 400 V_{pp}.

The input to the operational amplifier can be generated by a Digital-to-Analog Converter (DAC). The DAC can either be a part of the microcontroller forming the general control block of the system or added as a separate component.

The operational amplifier is supplied with fixed, symmetrical ± 70 V generated by a flyback converter with two identical secondary windings. Adjustment of the output voltage is done through a digital potentiometer in the feedback path of the operational amplifier and controlled by the microcontroller.

The greatest challenge in the described design is the selection of a correctly dimensioned, commercially available transformer for the output stage. Standard, off the shelf transformers are only available for a limited voltage and frequency range. Key characteristics of a transformer are the number of windings on each side and the type and form of the core material. Equations 2.14 and 2.15 show the relationship between the core material (maximum magnetic flux density $B_{\text{max,core}}$ and core cross-section A), number of windings (N), voltage (V) and frequency ($1/t$)):

$$\Phi = \frac{V \cdot t}{N} \tag{2.14}$$

$$B = \frac{\Phi}{A} = \frac{V \cdot t}{N \cdot A} \leq B_{\text{max,core}} \tag{2.15}$$

The minimum number of windings and core cross section depends on the maximum peak-to-peak Voltage (400 V_{pp}) and minimum frequency of 10 Hz.

A quote from a manufacturer of custom transformers contained a solution weighting about 30 kg to be able to cover the whole frequency range down to 10 Hz. This solution is unsuitable both in handling of the final device and price. Therefore, building a system utilizing an output transformer to push the generated output voltage to the required output voltage level is not possible.

Despite the fact that it is not possible to physically produce transformers working for the required frequency range for small electronic devices, a transformer would not be able to propagate a low frequency square wave from the input to the output. This is rooted in the fact that low frequency square waves can not be modeled as solely AC signals in practice, but contain a static DC component once the signal reaches the target voltage level. Transformers on the other hand can only propagate AC signals.

2.4.4 High Voltage Operational Amplifier

Not being able to cover the frequency range with a practically implementable inductive component fosters the idea to replace the output transformer with an active high-voltage stage.

A design following this approach incorporates an integrated operational amplifier being extended by a high voltage output stage as part of the feedback path of the integrated operational amplifier. Therefore, the integrated operational amplifier regulates the output stage and ensures a stable signal at the output. Furthermore, the operational amplifier does not need to sustain or provide high voltages and can be a standard operational amplifier. This design requires two separate symmetrical voltages, one for the operational amplifier and one for the high-voltage output stage. Both symmetrical voltages need to be provided by a power supply circuit on the to be designed board.

Components and their interconnections being part of a design following the described design are shown in figure 2.15:

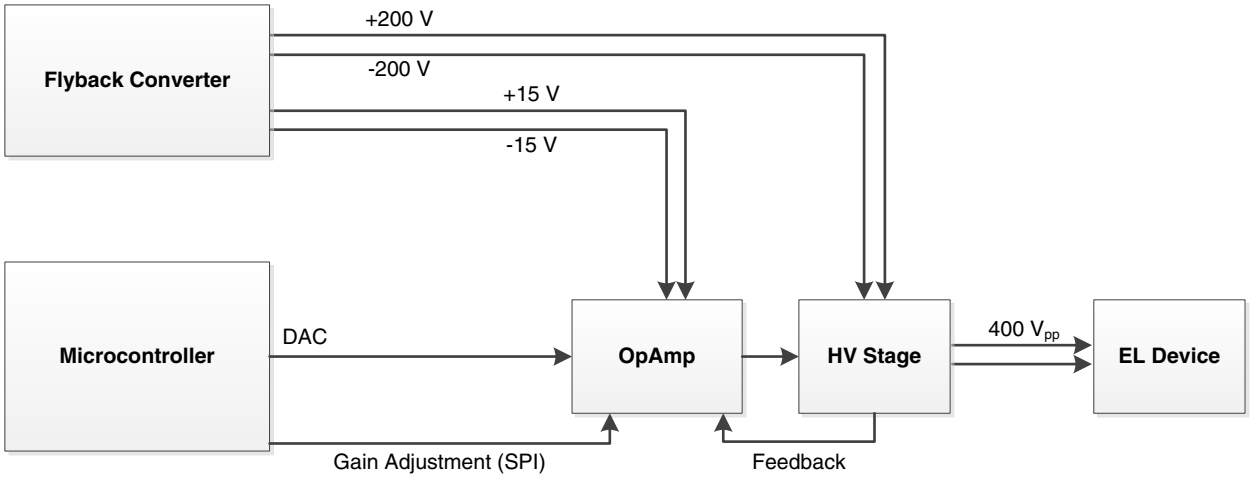

Figure 2.15.: Design featuring an high voltage output stage.

A thorough analysis of this solution showed that it is possible to implement a device following this approach. With all previously discussed designs having major drawbacks or constraints which can not be implemented in a practical solution, a design composed of a high-voltage output stage driven by an integrated operational amplifier is chosen as general approach for building a system implementing the requirements given for this project.

The next chapters will therefore give detailed information and analysis of this design, the parameters, and the process leading to the final implementation.

3 Design

This chapter describes the design and functionality of the building blocks composing the implemented high-voltage signal generator. The main focus of this chapter is on the driver board design while the design of the controller board is described in section 3.6.

Figure 3.1 shows a block diagram of the components of the driver board, illustrating the overall composition of the distinct blocks and connections between the different parts. The signal flow path (signal generation) in the diagram is, from left to right, made up of a control block providing overall control over the functionality of the system (described in section 3.5), an operational amplifier with high-voltage output stage (section 3.1), a current sensing circuit for RC time constant measurements of the connected device at the output (section 3.2) and dedicated voltage supply blocks for high- and low voltages (section 3.3).

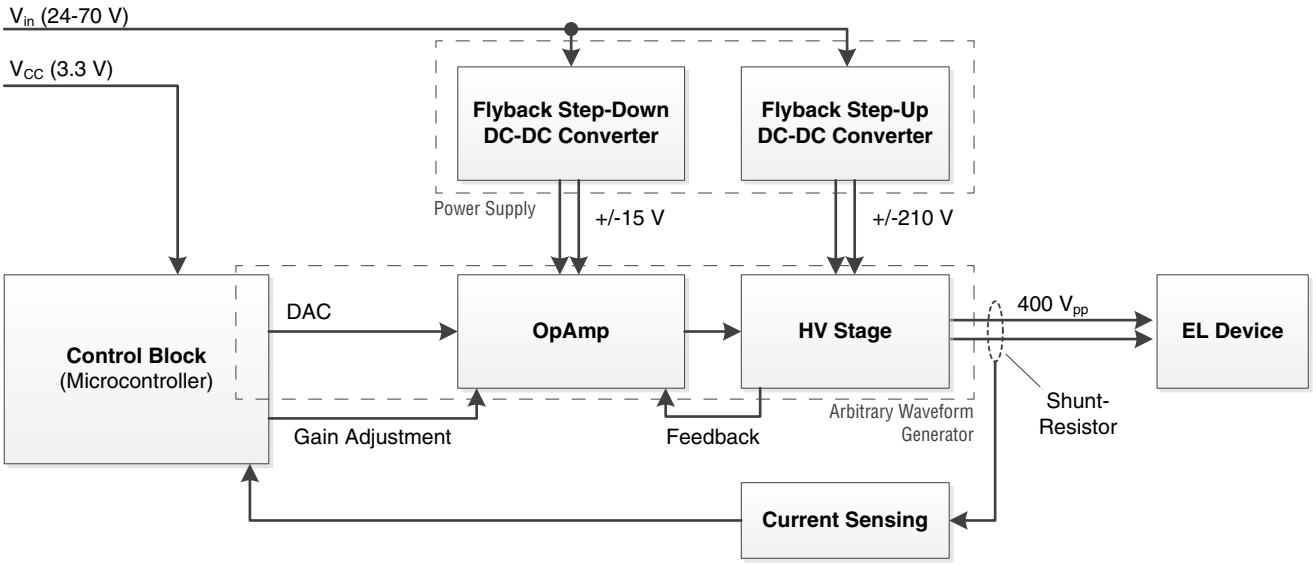

Figure 3.1.: Block diagram containing all components of the high-voltage signal generator.

The system design is described in the following sections in a top-down approach, starting at the essential core of the system for meeting the specified requirements (waveform generation), followed by the surrounding system blocks, for which requirements are deducted from their purpose of providing functionality to the waveform generator block.

3.1 Arbitrary Waveform Generator

The waveform generator consists of two functionally different blocks: a DAC generating arbitrary periodical waveforms and an operational amplifier with high-voltage output stage, transforming the logic level input signal to the desired high-voltage output signal. The DAC circuit as a part of the control logic is discussed in section 3.5. For the following section the only relevant and essential property of the DAC is the output voltage range from 0 to 3.3 V.

The design concept for an operational amplifier incorporating a high-voltage output stage is based on a "±120 V Swing Booster" circuit, published by *Texas Instruments* in an application note titled "Op Amp Booster Designs" [9] and shown in figure 3.2. In this design one output pin is tied to ground while the other can be driven to any voltage between −120 V and +120 V. The voltage amplification itself is done in the second stage (Q3 and Q4) while the third and fourth stage provide current amplification to drive larger loads.

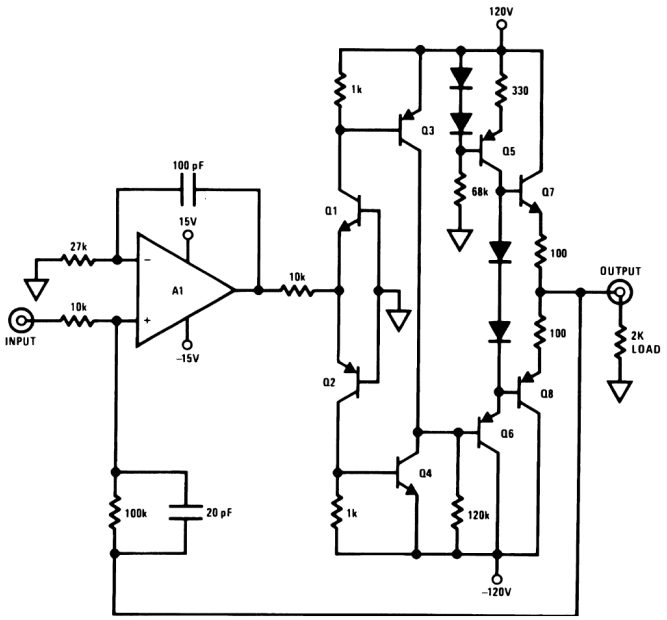

Figure 3.2.: Original "±120 V Swing Booster" circuit by *Texas Instruments* [9, figure 6, p. 8].

The feedback is returned to the positive input terminal of the integrated operational amplifier, because the high-voltage output circuit inverts the input signal in the second stage (Q3 and Q4) [9]. The gain factor is set by the two resistors connected to the positive input terminal of the operational amplifier. In the shown circuit the gain factor is fixed to 10. AC coupling the operational amplifier's output to the negative input provides "circuit dynamic stability" [9].

Using this "Swing Booster" circuit as basis for the designed system, a number of requirements for the design of this block can be extracted: To amplify a 3.3 V_{pp} input voltage to 400 V_{pp} a maximum gain factor of 121 is required. The output voltage should also be adjustable to very low voltages (ideally zero), therefore a mechanism to dynamically adjust the gain factor is required. Furthermore, the 0 to 3.3 V input signal needs to be balanced to achieve a symmetric ±200 V output signal. The transistors in the second to fourth output stage are connected with the emitter or collector pin to either supply voltage rails while the respective other pin is connected to the output signal path. These transistors must therefore sustain collector-emitter voltages (V_{ce}) of atleast 400 V.

The design of the final circuit meeting the general system requirements and the listed requirements deducted from the chosen topology can be divided into three problems discussed in the following sections:

1. Balancing the input signal (section 3.1.1)
2. Dynamic adjustment of the gain factor (section 3.1.2)
3. Design of the output stage for 400 V_{pp} output signals (section 3.1.3)

3.1.1 1. Balancing the Input Signal

Balancing the input signal can be accomplished by following two general approaches: the first one is to provide a DC bias of 1.65 V to the operational amplifier which is incorporated as negative offset in the operation of the amplifier. A second approach is to use an AC coupling capacitor to connect the 3.3 V_{pp} input signal to the operational amplifier stage.

The second approach is from a design perspective a simpler solution and can be implemented as a high-pass filter. The cutoff frequency of this high-pass filter needs to be low enough to allow sine waves with the minimum required frequency (10 Hz) to pass through the filter without major amplitude reduction. The lower-end is not limited, because the purpose of the filter is to block only the DC bias of the signal. Figure 3.3 shows a high-pass filter implementation with a cutoff frequency of 3.98 Hz.

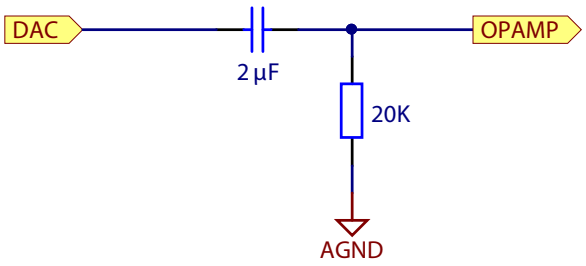

Figure 3.3.: High pass filter for AC coupling of the DAC to the operational amplifier input.

The amplitude of a 10 Hz sine wave passing through this filter is reduced to a value of 0.72-times the original amplitude. This value can be improved by using larger values for the resistor or capacitor composing the filter, but increasing these values also imposes side effects. A larger capacitance in the filter requires higher slew rates of the DAC generating the signal which is especially important for generating high frequency square waves. A higher resistance in the filter leads to higher settling times at system start, due to the longer time it takes until the input signal is centered around 0 V (ground). Therefore, the shown high-pass filter is used as a compromise between low-frequency operation and high-frequency performance.

The feedback of the high-voltage output stage is returned to the same input pin of the operational amplifier to which the input signal is fed. Therefore, the shown high-pass filter, which is used to achieve AC coupling of the input signal and the operational amplifier would interact with the feedback network of the operational amplifier and vice versa. To decouple both functional blocks, a second operational amplifier stage prior to the main operational amplifier is introduced. Figure 3.4 shows this operational amplifier with the supporting circuit in a non-inverting configuration and a gain factor of 2.

The need for a second operational amplifier suggests the usage of an IC with two integrated operational amplifiers. Therefore, the `LT1678` by *Linear Technology* is selected for the design. The `LT1678` is a dual rail-to-rail low noise and high precision operational amplifier with up to ±18 V supply voltage, 6 V/μs slew rate and 20 MHz gain bandwidth product [10]. Operational amplifiers by *Linear Technology* are also well supported by their *SPICE* software *LTSpice*, which allows extensive simulation of circuits containing operational amplifiers sold by *Linear Technology*.

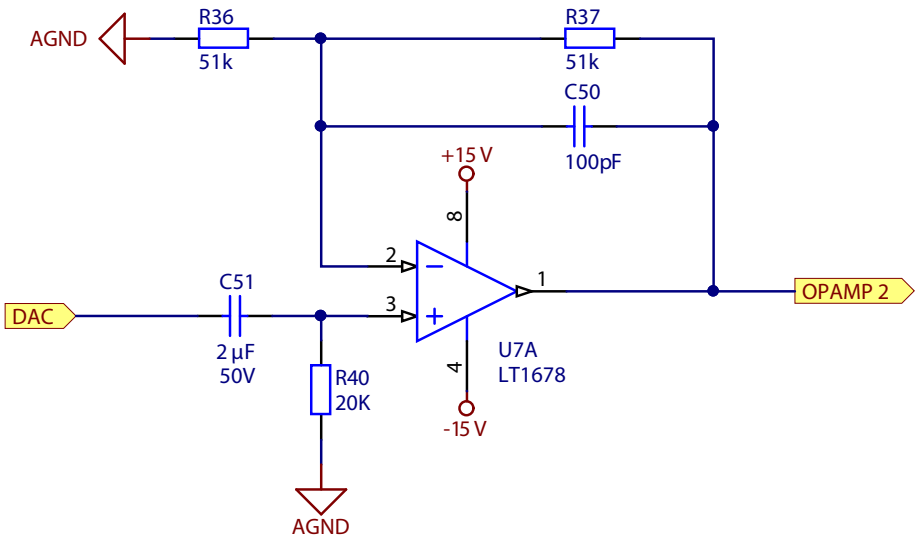

Figure 3.4.: A second operational amplifier is used to decouple the input balancing circuit from the main operational amplifier.

Using a high-pass filter to remove the DC bias from the input signal works for high frequency signals, but results in an effect not covered by the high-frequency model of the described circuit: Square waves with low frequencies result in an amplitude decay shortly after the high or low level of the signal is reached (figure 3.5). This effect is based on the fact that no high frequency components are contained in the input signal during the short time frames right before the signal changes to the opposing voltage level. During this time frame the capacitor discharges through the resistor `R40`, which also results in a change in the output voltage of the operational amplifier.

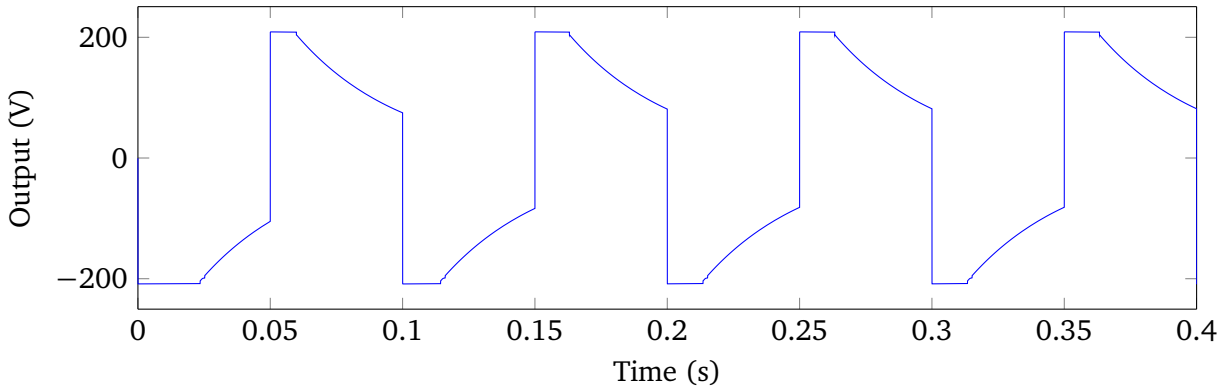

Figure 3.5.: Decay of a 10 Hz square wave.

By changing the values of the resistor and capacitor in the high-pass filter this effect could be minimized, but that would also impose other side effects as discussed before. The parameters of any passive filter circuit depend on the input frequency. Therefore, another solution needs to be implemented for this application, which has to work for a wide frequency range. In the introduction to the input signal balancing problem the incorporation of a DC bias in the operational amplifier circuit by means of a negative DC offset, is mentioned as another approach. This could be achieved by biasing the negative input terminal of the operational amplifier at 1.65 V. An implementation of this bias requires an additional resistor between the negative input of the operational amplifier and the supply voltage (3.3 V). This results in a star topology with the negative input terminal of the operational amplifier as center tap

which can not be canceled out (figure 3.4) and is therefore not mathematically solvable by common star-mesh-transformations.

A standard inverting amplifier circuit has one (the positive) terminal tied to *ground* and the other (negative) terminal connected to the input signal and feedback path [8, p. 553]. This yields the characteristic *inverting* operation mode, but is only a special application of the general circuit. The functionality of this circuit can, in a more general way, be described as a signal mirror with the reference (mirror point) set through the voltage at the positive input terminal. Figure 3.6 shows the general circuit of an inverting amplifier:

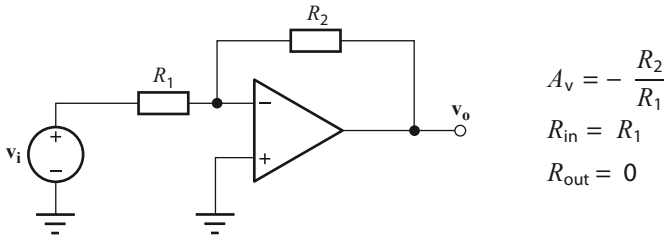

Figure 3.6.: Inverting amplifier circuit [8, figure 10.18, p. 553].

For the application of balancing a 0 to 3.3 V input signal around 0 V (ground) the potential of the positive input terminal must be set to a positive, fixed DC voltage. The calculation for this reference voltage (V_{ref}) at the positive input terminal is based on the following equation for the output voltage assuming a given, negative amplification factor A_V:

$$V_{out} = A_V \cdot V_{in} - (A_V - 1) \cdot V_{ref} \tag{3.1}$$

Setting V_{ref} to 0 V yields the commonly known output voltage equation for inverting amplifiers. The requirement for a balanced output signal yields the following equation, stating that the minimum output voltage is equal to the maximum output voltage with inverted algebraic sign:

$$V_{out,max} + V_{out,min} = 0 \tag{3.2}$$

Combining equations 3.1 and 3.2 yields a formula for calculating the reference voltage V_{ref}. Due to the inverting behavior of the operational amplifier, V_{in} must be substituted by $V_{in,min}$ to calculate $V_{out,max}$ and vice versa for $V_{out,min}$:

$$A_V \cdot V_{in,min} - (A_V - 1) \cdot V_{ref} + A_V \cdot V_{in,max} - (A_V - 1) \cdot V_{ref} = 0 \tag{3.3}$$

$$A_V \cdot (V_{in,min} + V_{in,max}) - 2 \cdot (A_V - 1) \cdot V_{ref} = 0 \tag{3.4}$$

After substituting A_V with the desired amplification factor of -2, $V_{in,max}$ with 3.3 V, $V_{in,min}$ with 0 V the equation results in a reference voltage V_{ref} of 1.1 V:

$$V_{\text{ref}} = \frac{A_V \cdot \left(V_{\text{in,min}} + V_{\text{in,max}}\right)}{2 \cdot \left(A_V - 1\right)} = \frac{-2 \cdot (0\,\text{V} + 3.3\,\text{V})}{2 \cdot (-2 - 1)} = \frac{3.3\,\text{V}}{3} = 1.1\,\text{V} \tag{3.5}$$

Applying the calculated reference voltage to the positive input terminal, by using a 2:1 voltage divider between $V_{\text{CC}} = 3.3$ V and 0 V (ground) build from two resistors, leads to a non-zero output of the operational amplifier block when no input signal is supplied to the operational amplifier (sourced in the DAC). This results in a static output voltage of +200 V at the output terminals of the system, when it is in static standby state. This can be circumvented by not using a static voltage divider, but supplying the reference voltage for the positive input terminal from another DAC channel. A 20 kΩ pull-down resistor ensures a safe default state, when the DAC is not operational.

Figure 3.7 shows the final design of the first operational amplifier stage, based on the concept of an inverting amplifier with a fixed amplification factor of −2 and a dynamically controllable DC offset voltage and reliable *off* state:

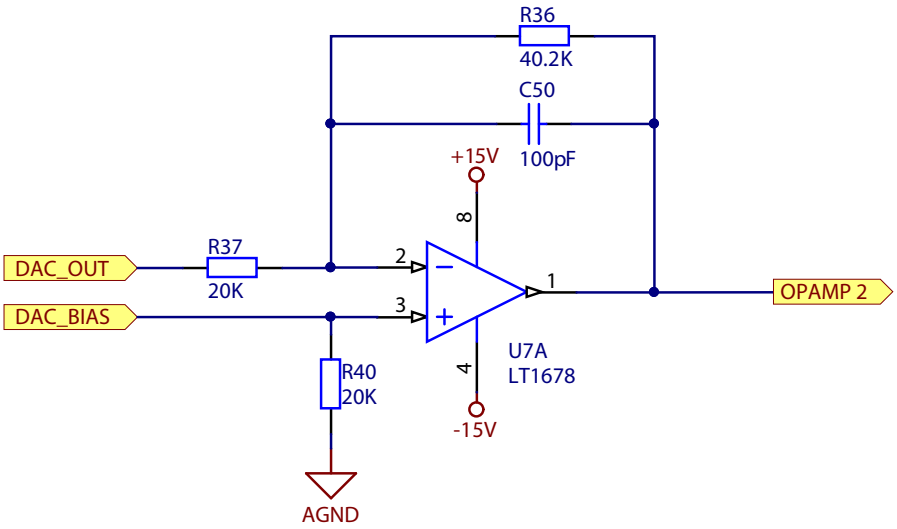

Figure 3.7.: First stage of the operational amplifier block with controllable DC bias for balancing logic level input signals.

A side effect of using an inverting amplifier in the shown configuration for the input balancing stage is, that it also acts as a low-pass filter rejecting high-frequency noise generated by the DAC. The corner frequency of the low-pass filter is determined by R_{36} and C_{50} [8, p. 578] and set to about 40 kHz:

$$f_c = \frac{1}{2\pi \cdot R_{36} \cdot C_{50}} = \frac{1}{2\pi \cdot 40.2\,\text{k}\Omega \cdot 100\,\text{pF}} = 39.59\,\text{kHz} \tag{3.6}$$

The first two harmonics of a 5 kHz square wave pass this filter, and it has therefore almost no visible effect on the output signal while rejecting higher frequencies being present as superimposed noise on top of the intended signal.

3.1.2 2. Adjustable Gain Control

The first stage of the waveform generator block is designed to balance a 0 to 3.3 V input signal around 0 V and has an amplification factor of 2. Therefore, the output of this stage provides a ±3.3 V signal to the next stage. This next stage in the signal chain is the actual high-voltage amplifier stage based on the circuit by *Texas Instruments* as shown previously in figure 3.2.

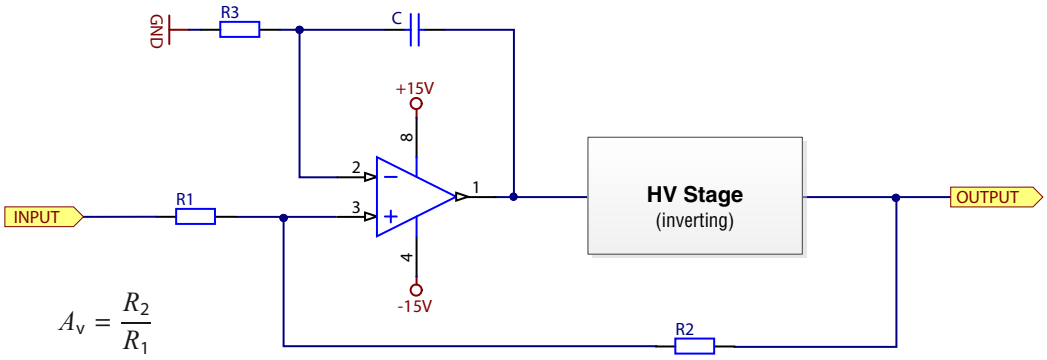

Figure 3.8.: Gain adjustment of the high-voltage operational amplifier stage.

The usage of the operational amplifier in this circuit block does neither follow the model of an inverting amplifier nor is it in the form of a non-inverting amplifier. A comparison of the previously shown standard inverting amplifier (figure 3.6) and the used circuit (figure 3.8) reveals, that it has the form of an inverting amplifier, but with swapped positive and negative inputs of the integrated operational amplifier. This is due to the inverting behavior of the high-voltage amplification stage following the integrated operational amplifier. The gain factor A_V is therefore calculated by using the equation for inverting amplifiers [8], although the inputs to the operational amplifier are swapped:

$$A_V = -\frac{R_2}{R_1} \tag{3.7}$$

To be able to adjust the gain of this amplifier stage, the value of one of the resistors needs to be adjustable by the digital control circuit. This requires the usage of an *digital potentiometer*. Key characteristics of the required digital potentiometer are the possibility to work with high voltages above standard 5 V Transistor–transistor logic (TTL) levels, high precision for fine control of the gain factor and dual supply voltage capability for the usage with feedback signals balanced around 0 V (ground).

Browsing the catalogs of large, commonly known component distributors showed that the requirement for high precision with less than 10 % variance in the controlled value restricted viable solutions to products by *Analog Devices*. The requirement for dual supply voltage operation above and beyond ±5 V narrowed down the results to the `AD529x` series by *Analog Devices*. The used `AD5293` is a single-channel, 10-bit digital potentiometer with 1% nominal resistor tolerance, Serial Peripheral Interface (SPI) and dual-supply operation from ±9 V to ±16.5 V [6]. It therefore can be used with the same dual power ±15 V voltage supply required for the integrated operational amplifier. The `AD5293` is available with 20, 50 and 100 kΩ nominal resistor value.

Resistor R_2 in the feedback path needs to sustain ±200 V at the pin connected to the output of the system. It is therefore not possible to replace it with a digital potentiometer having a maximum pin voltage of ±16.5 V. The only option to stay within the maximum voltage boundaries is to place the digital potentiometer at the position of R_1, because its pin-to-ground voltage must never exceed ±16.5 V to prevent damaging the circuit.

The positive input of the second stage of the integrated operational amplifier is connected to ground by using a 20 kΩ resistor (R_3 in figure 3.8). Therefore, the operational amplifier tries to drive its output to the respective voltage required to match the potential at its negative input to ground as well. This leads to a (virtual) ground potential at the connection of R_1 and R_2 and the current through both resistors has to cancel out:

$$\frac{V_{\text{in}}}{R_1} = \frac{V_{\text{out}}}{R_2} \tag{3.8}$$

Maximum input and output voltages define the minimum ratio of the resistors to

$$\frac{R_2}{R_1} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{200\ \text{V}}{3.3\ \text{V}} = 60.\overline{60}. \tag{3.9}$$

This equation shows that a minimum value for R_1 is required to stay within the bounds of the target output voltage. Replacing R_1 with a digital potentiometer would therefore waste the lower range of the adjustable value range. Additionally an error in the software controlling the potentiometer value could lead to hazardous output voltages outside of the specified range for which the system is designed. Therefore R_1 is split into a fixed resistor R_{low} setting the maximum gain of the system and an adjustable potentiometer R_{pot} to control the gain below this fixed point of maximum gain. The resulting circuit is shown in figure 3.9:

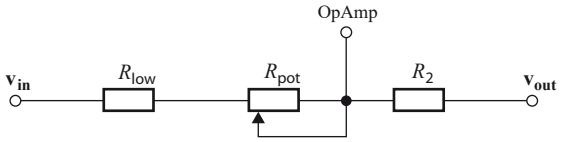

Figure 3.9.: Feedback network of the high-voltage operational amplifier stage.

Setting R_{low} to 5 kΩ results in a value for R_2 of

$$R_2 = \frac{200\ \text{V}}{3.3\ \text{V}} \cdot 5\ \text{k}\Omega = 303.\overline{03}\ \text{k}\Omega. \tag{3.10}$$

For the implementation of the design, R_2 is split into three series resistors with values of 100 kΩ and two times 102 kΩ to reduce the voltage drop and therefore the power dissipation for the individual resistors. The resulting resistance of 304 kΩ yields a current across the resistors of 0.66 mA.

Two capacitors in parallel to this resistor chain (figure 3.11) provide dynamic stability. Their values are set to 7 pF and 10 pF which results in maximum slope but avoids overshoot spikes for square wave

signals. The values were determined by running SPICE simulations of the complete circuit containing the operational amplifiers.

The digital potentiometer IC is available in three variants with 20 kΩ, 50 kΩ and 100 kΩ nominal resistance. A high value of the adjustable resistor yields a low minimum gain of the output stage and therefore a wide gain adjustment range, but also reduces the linearity of the adjustable gain. Equation 3.11 shows this correlation:

$$V_{\text{out}} = \frac{304\ \text{k}\Omega}{5\ \text{k}\Omega + R_{\text{pot}}} \tag{3.11}$$

The different effects of choosing one of the variants of the digital potentiometer is visualized in figure 3.10 which shows the minimum achievable output voltage and the linearity of the system in between the maximum and minimum output voltage:

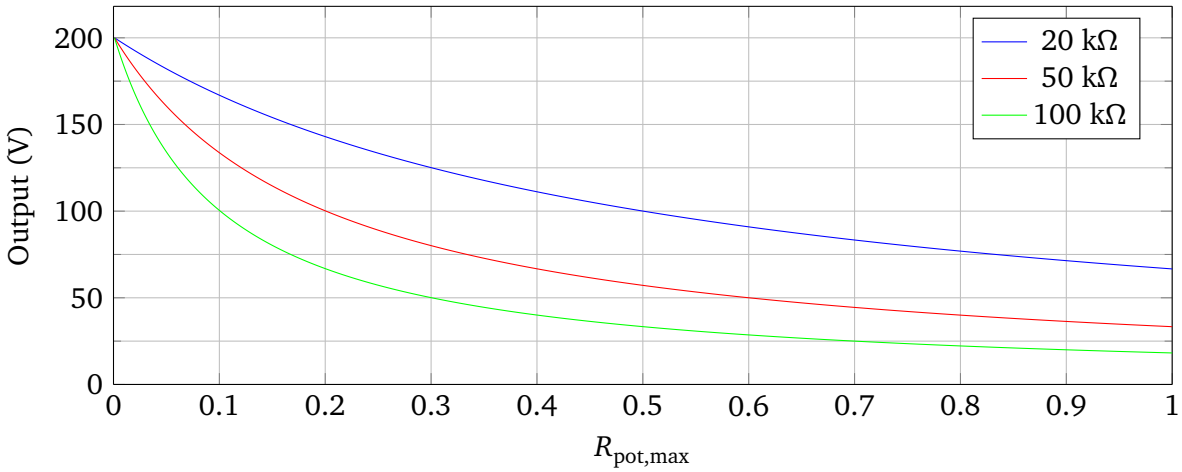

Figure 3.10.: Output voltage in dependency of the digital potentiometer value.

Another way to reduce the minimum output voltage of the system is to reduce the amplitude of the signal generated by the DAC and used as input to the operational amplifier stage. This is easily achievable by a respective software implementation controlling the system. Therefore the 20 kΩ variant of the digital potentiometer is used for this design to achieve maximum linearity of the adjustable gain. This yields a minimum gain of the output stage of

$$\frac{304\ \text{k}\Omega}{25\ \text{k}\Omega} = 12.16, \tag{3.12}$$

which corresponds to a minimum output voltage of 40.13 V for a 3.3 V amplitude input signal.

Resistor R_{45} and capacitor C_{52} at the negative input of the operational amplifier form an integrator [8, p. 582] to provide stability to the circuit by shortcutting high frequencies to the negative input of the operational amplifier.

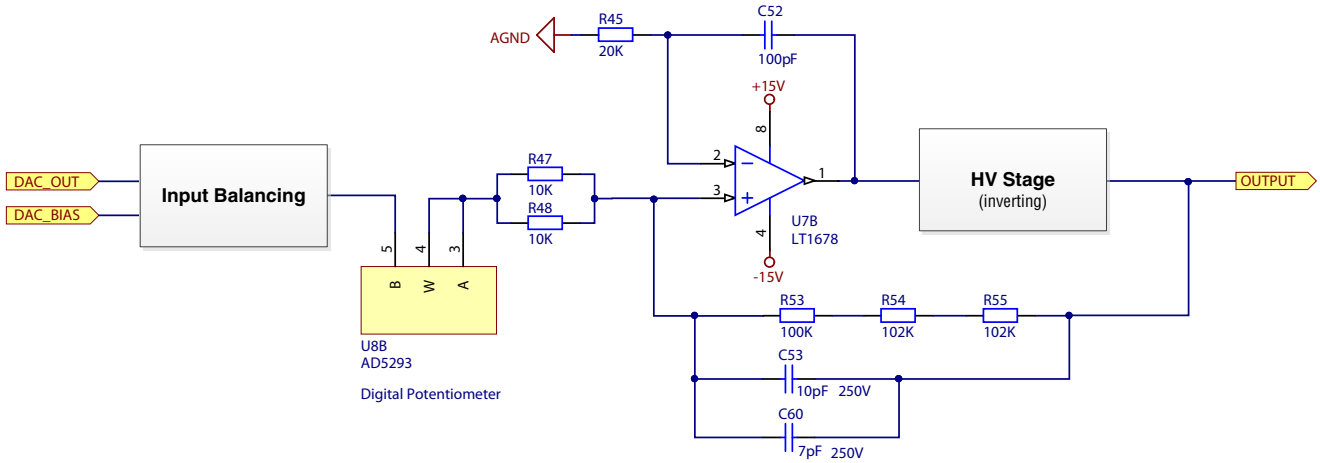

Figure 3.11.: First stage of the operational amplifier block with controllable DC bias for balancing logic level input signals.

3.1.3 3. High-Voltage Output Stage

A high-voltage output stage transforms the output of the operational amplifier to the required ±200 V signal at the output of the system. The design of this output stage is based on the circuit published by *Texas Instruments* (figure 3.2), but adapted to work not only with ±120 V output voltages, but with ±200 V as required. Therefore the Bipolar-Junction Transistors (BJTs) used in this design have to sustain collector-emitter voltages (V_{ce}) of at least 400 V. To achieve symmetrical behavior of the system for positive, as well as negative voltages, complementary PNP/NPN transistors are preferred for this design. The current drive capability of the high-voltage signal generator is specified to 300 mA. The last two transistors of the output amplifier block are providing the current for driving loads connected to the output terminals and therefore need to have a current rating of atleast 300 mA. The only BJTs fulfilling these requirements for high-voltage and current capability plus being designed for complementary NPN/PNP usage are the `STR1550` (NPN) and `STR2550` (PNP) transistors by *STMicroelectronics*. The `STR1550` and `STR2550` are designed for complementary usage, are rated for a V_{ce} of 500 V, have a rated current drive capability of 500 mA [11] [12], and are therefore used in this design. Although only the last two stages of the output amplifier block are required to provide high currents, the selected transistors are used for all stages of the output stage to minimize the number of different components required to build the system.

Figure 3.12 shows the modified design of the output amplifier block containing the `STR1550` and `STR2550` BJTs. Compared to the original design, transistors R_{51} and R_{41}/R_{42} are increased in size to minimize the dissipated power in these components. Splitting the upper resistor into two parallel resistors (R_{41} and R_{42}) is done for the same reason. To provide the required current for charging/discharging of the capacitive load connected to the output of the system as fast as possible, a 10 nF and a 100 nF capacitor are placed close to the collectors pins of both transistors driving the output load on the supply rails. The supply voltage is increased to ±210 V to provide an additional margin compared to the required output voltage of ±200 V.

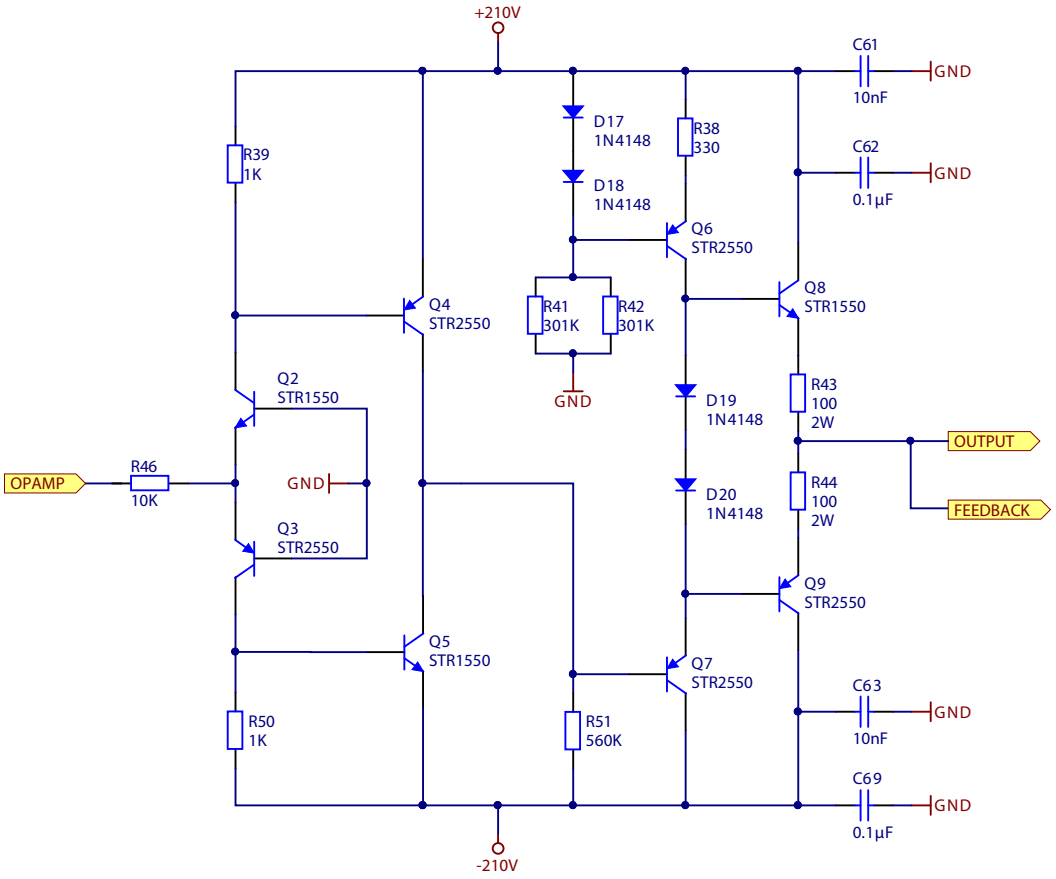

Figure 3.12.: Initial design of the high-voltage output stage of the operational amplifier block.

The voltage amplification to the target output voltage is accomplished by the second stage (*Q4* and *Q5*) of the output amplifier block. The first stage (*Q2* and *Q3*) controls the base current of the two complementary transistors in the second stage, based on the input signal coming from the integrated operational amplifier. Stage three (*Q6* and *Q7*) and stage four (*Q8* and *Q9*) provide the required current for driving the load connected to the output. The diodes *D17* to *D20* are required to provide bias for the transistors to limit crossover distortion.

A first prototype was built based on the design as shown in figure 3.12 and proved general functionality of the system, but also showed that the four transistors of the last two output stages heated up to around 93 °C (shown in figure 3.13).

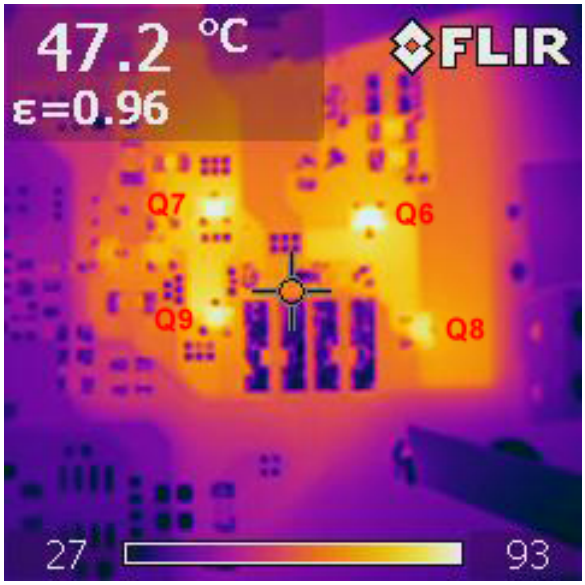

Figure 3.13.: Infrared image of the output stage build for a first prototype.

The findings gained from tests with a prototype based on the initial design were incorporated in a second version of the design. Overheating of the output stage transistors could be fixed by using transistors with higher current drive capability, but no commercially available transistors for the required high-voltage, complementary design with higher current drive exist. Therefore, the transistors in the output stage are doubled. To ensure an equally shared load across the doubled transistors at each point in the circuit, 1 Ω emitter resistors are added. The current through these resistors leads to a voltage drop at the emitter pin of each transistor depending on the current through this single transistor. The voltage drop at the emitter pin leads to a reduced base-emitter voltage (V_{be}), which itself leads to a reduced current gain of the transistor. The addition of the emitter resistor should therefore lead to balanced currents through the doubled transistors.

The resulting final high-voltage output stage circuit is included in the appendix (section B.2.1, schematic sheet 8).

3.2 Output Signal Measurement

To measure the RC constant of the EL device connected to the output of the system, the current draw can be measured using a combination of a shunt resistor and another operational amplifier. The operational amplifier is required to increase the very small voltage drop over the shunt resistor to a reliably measurable and ascertainable voltage by an ADC as part of the digital control circuit. The operational amplifier needs to have a very high common mode rejection ratio and must be able to work with high, dual (bidirectional) voltages at the input terminals. For this application special current sensing amplifiers are available by integrated circuit manufacturers. The *Texas Instruments* `LMP8603` current sensing amplifier works with a common offset voltage range from −22 V to +60 V by using a single 5 V power supply and can sense bidirectional current flows [13]. It is therefore well suited for the described application and used in the design of the system.

A 0.1 Ω shunt resistor leads to a voltage drop of 30 mV at an absolute maximum current of 300 mA. This voltage drop is insignificant compared to the maximum output voltage of 200 V, yet large enough for a current sense amplifier.

The common mode input voltage to the current sense amplifier must not exceed the specified −22 V to +60 V, but the measured voltage ranges between ±200 V. The connection from the shunt resistor to the current sense amplifier must therefore feature a voltage divider network. It is critical that the voltage divider ratio to both inputs is exactly the same. Variants in the resistor values due to production tolerances would otherwise lead to a constant offset voltage at the output of the current sense amplifier. To accomplish this, a trimmer is used as a variable value resistor in one of the two voltage divider circuits to allow in-circuit calibration of the system.

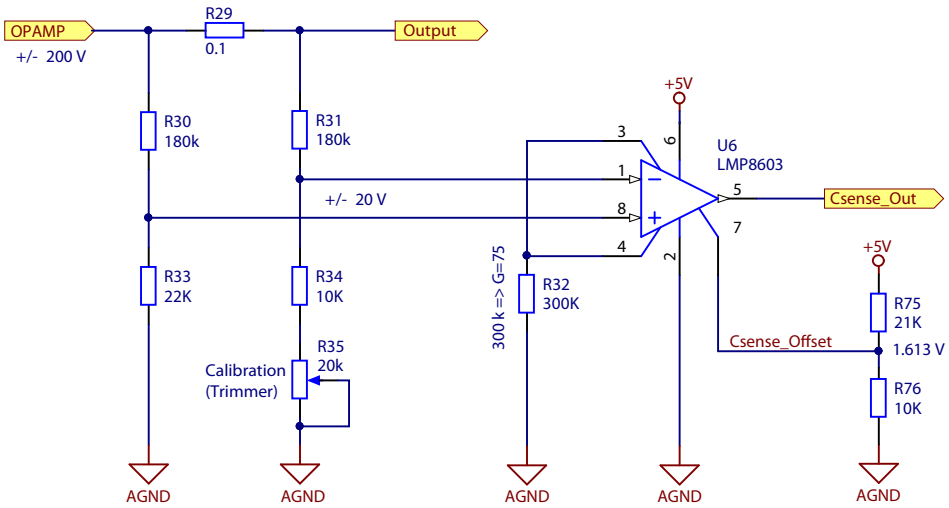

Figure 3.14.: Current sense amplifier with support circuitry for (bidirectional) output current measurement.

Beside the maximum input voltage of −22 V and +60 V, a chosen maximum current through the resistor network of 1 mA forms the basis for the design of the resistor network forming the voltage divider. The current limit results in a minimum series resistance of 200 kΩ. Therefore, the voltage divider network is build from a 180 kΩ and a 22 kΩ resistor as shown in figure 3.14. This adds a small safety margin and results in a maximum common mode voltage of

$$\pm 200\ \text{V} \cdot \frac{22\ \text{k}\Omega}{180\ \text{k}\Omega + 22\ \text{k}\Omega} = \pm 21.78\ \text{V} \tag{3.13}$$

at the current sense amplifier input terminals.

The gain of the differential input voltage is fixed to 75 by a 300 kΩ resistor at the respective IC pin [13]. Therefore, a 300 mA output current results in a 30 mV voltage drop over the shunt resistor and is amplified to an output of 2.25 V at the current sense amplifier. With one output terminal of the system connected to ground and the other output terminal ranging between −200 V and +200 V, a bidirectional current flow occurs through the shunt resistor. A negative offset voltage between the input terminals of the current sense amplifier would lead to a negative output voltage, but is capped to 0 V by the limited supply voltage range. To measure bidirectional currents, an offset voltage needs to be set at the respective pin of the current sense amplifier. The calculated 2.25 V maximum output voltage covers less than the lower half of the supply voltage, which would allow an offset voltage of 2.5 V for the amplifier output. But the connected digital control circuit containing the ADC works at a supply voltage of 3.3 V. The output voltage of the current sense amplifier must not exceed this voltage. Therefore a voltage offset of 1.613 V is designed into the circuit using a voltage divider formed by a 21 kΩ (R_{75}) and a 10 kΩ (R_{76})

resistor. This reduces the maximum mensurable output current to 215 mA. If higher currents have to be measured, the lower resistor (R_{76}) can be replaced with a 0 Ω jumper. This modification of the circuit eliminates the possibility to measure bidirectional currents.

Two decoupling capacitors with a value of 100 nF and 10 μF are placed at the power supply pins of the current sense amplifier, but not shown in figure 3.14.

The `LMP8603` current sense amplifier works with supply voltages down to 3.0 V, but the input common mode voltage range covers −22 V to +60 V only when operated with 5 V supply voltage [13, p. 3, p. 5]. This induces the requirement of a 5 V supply voltage, which has to be generated by the power supply circuitry on the driver board.

3.3 Power Supply

The power supply circuit needs to generate output voltages with +210 V, −210 V, +15 V, −15 V, +5 V and +3.3 V from a supplied DC input voltage in the range between 24 V and 70 V.

To generate ±210 V a step-up converter design is required, the other voltages need a step-down converter design. +3.3 V are also required for the microcontroller on the controller board and the required current can be supplied by a single step-down converter circuit for all connected controller and driver boards. Therefore, the power supply is split in three distinct circuits: one high-voltage step-up converter for supplying ±210 V on the driver board, one step-down converter for supplying ±15 V and +5 V on the driver board and one step-down converter on the controller board for supplying +3.3 V for all digital components on the controller board and the connected driver boards.

The requirement for symmetrical ±210 V and ±15 V suggests the implementation of DC-DC converters in a flyback design.

Flyback converters can be implemented in step-up or step-down configuration and feature a transformer with one primary and one or multiple secondary windings as inductive element. They are often used to provide isolation between input and output voltages but are not limited to this application and can be used in a non-isolated circuit, too.

3.3.1 High-Voltage Flyback Step-Up Converter

The three key components in a flyback DC-DC converter are the PWM controller IC, the switching transistor and the transformer.

The PWM controller IC must be able to cover the whole input voltage range and should work with a switching frequency satisfying the Voltage-second constant of the transformer. Especially the constraint on the input voltage range limits the available solutions greatly. But the `LM5020` "13-100V Wide Vin, Current Mode PWM Boost Controller" IC by *Texas Instruments* fulfills these requirements and is therefore used in the high-voltage power supply circuit.

The reference feedback voltage (see section 2.4.1) of the controller IC is 1.25 V. To achieve a stable feedback voltage to the feedback pin, the voltage divider is designed for about 0.5 mA current. Choosing R_1 to 402 kΩ and R_2 to 2.4 kΩ gives a ratio of 167.5 and leads to a nominal output voltage of 210.63 V. The current across the voltage divider can be calculated to 0.519 mA.

Instabilities in the error amplifier output (section 2.4.1) can be stabilized by connecting an external compensation network to the `COMP` pin of the IC. The recommended network topology and component values are provided in the datasheet of the controller IC [14, p. 9].

Figure 3.15 shows the feedback and compensation network of the controller IC:

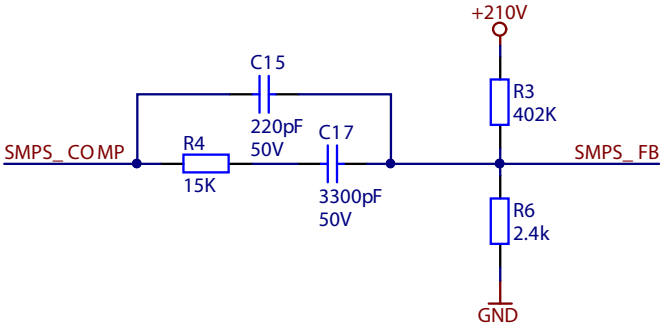

Figure 3.15.: Feedback and compensation network of the high-voltage step-up converter.

For a consistent step-up operation over the whole input voltage range, the primary-secondary windings ratio must not exceed 1:3. The transformer must also contain two identical secondary windings and has to be able to supply the required output current of 300 mA.

The transformer `750311889` by *Würth Electronic* fulfills these requirements with a primary inductance (L) of 37.0 μH, a saturation current (I_{Lpk}) of 2.95 ADC, a turns ratio of 1:2.5 and two identical secondary windings. The *voltage-second* constant of this transformer can be calculated to

$$V \cdot t = L \cdot I_{\text{Lpk}} = 109\ \mu\text{V s}. \tag{3.14}$$

With an assumed efficiency η of 90%, a turns ration n of 2.5 and the minimum input voltage (V_{in1}) of 24 V, the maximum duty cycle (D) can be calculated to 0.742857:

$$D = 1 - \frac{V_{\text{in1}} \cdot \eta \cdot n}{V_{\text{out}}} \tag{3.15}$$

The `LM5020` controller IC is available in two version: `LM5020-1` with a maximum duty cycle of 80% and `LM5020-2` with a maximum duty cycle of 50% [14]. The `LM5020-1` is capable to operate with the calculated duty cycle of about 74% and therefore chosen for this design. Combining formulas 3.14 and 3.15 results in the minimum switching frequency f_{min}:

$$f_{\text{min}} = \frac{D \cdot V_{\text{in1}}}{VS} = 163\ \text{kHz} \tag{3.16}$$

The ripple current I_{ripple} is also a function of the switching frequency:

$$I_{\text{ripple}} = \frac{V_{\text{in1}} \cdot D}{f \cdot L} \tag{3.17}$$

Therefore the switching frequency was chosen above f_{min} and set to about 300 kHz. The frequency is set through an external resistor between GND and the RT pin of the controller IC and calculated according to formula 3.18 [14, p. 8].

$$R_T = \frac{1}{f \cdot 158 \cdot 10^{-12}} \tag{3.18}$$

Choosing R_T to 20 kΩ yields a switching frequency of 316.456 kHz.

This results in a ripple current (equation 3.17) of 1.52 A. The maximum switching current for an output current of 300 mA can be calculated to 6.59 A:

$$I_{\text{SW}} = \frac{1}{2} \cdot \frac{I_{\text{ripple}}}{1 + \frac{I_{\text{out}} \cdot n}{1-D}} \tag{3.19}$$

Beside the regulation through voltage feedback, the IC has a current sense feature to limit the maximum output current. The voltage is sensed using a shunt resistor. The threshold voltage for current limiting is 0.5 V [14, p. 8]. This results in a maximum shunt resistor value of 75.8 mΩ for the calculated maximum switching current. A value of 47 mΩ is chosen for this design to accommodate a buffer for the practical implementation. A low-pass filter consisting of a resistor and a capacitor is required to protect the current sense circuitry inside the controller IC from high frequency noise.

The controller IC requires an external capacitor at the SS pin for its internal slow-start feature. This capacitor provides a voltage ramp on power up and delays the start of operation of the controller IC. The value is chosen, according to the datasheet, to 10 nF.

The operating voltage for the internal circuitry of the controller IC is generated by an integrated linear voltage regulator. The integrated voltage regulator requires an external capacitor with a value of 1 μF at the VCC pin of the IC. For high input voltages the losses inside the integrated linear voltage regulator circuit increase. Providing an external voltage above 8 V and below 15 V [14, p. 7] switches the internal voltage regulator off and uses the provided external voltage. Therefore the +15 V output of the other power supply circuit is connected to this pin by using a diode.

Figure 3.16 shows the external support circuitry for the high-voltage step-up controller IC:

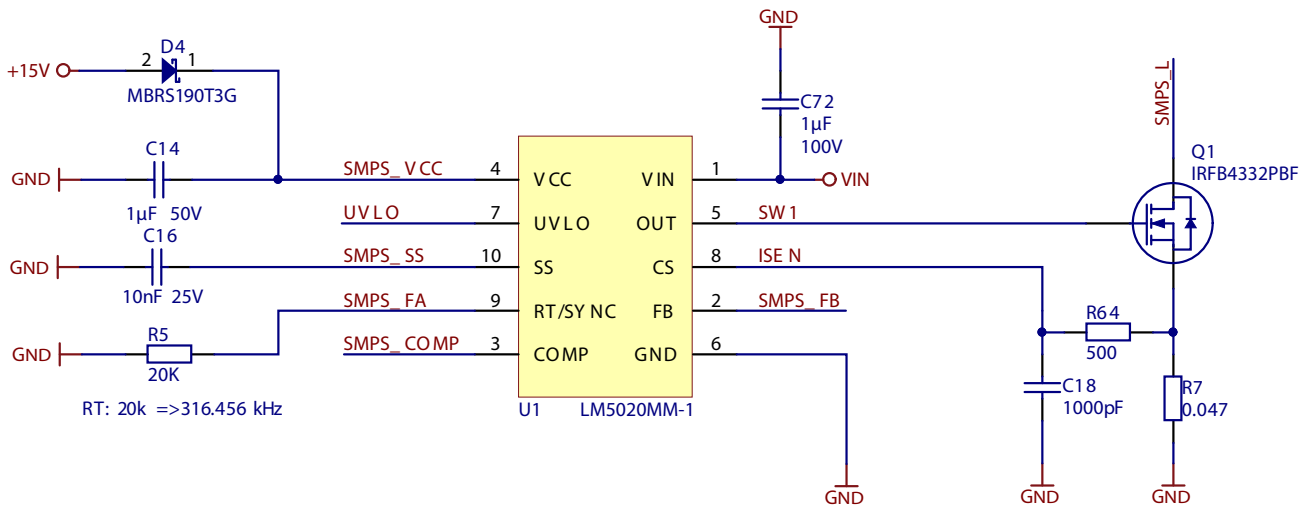

Figure 3.16.: External Circuitry for the High-Voltage Step-Up Converter.

The controller IC has an under-voltage lockout (UVLO) feature, stopping operation when the input voltage falls under a certain threshold. This feature can also be used to switch the controller IC on and off via an external control circuit. In this design activating and deactivating of the high-voltage power supply is done through the microcontroller based control circuit using the UVLO pin. A diode is used to protect the control circuit from hazardous high voltages caused by potential malfunctioning of the power supply circuit. A 20 kΩ pull-down resistor ensures a stable default state.

Figure 3.17 shows the UVLO circuitry:

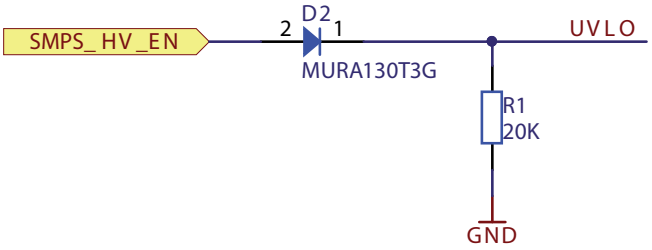

Figure 3.17.: On/Off control of the high-voltage power supply.

Selection of the switching transistor depends on two primary parameters: the maximum drain-source-voltage the transistor can sustain and the *ON* resistance of the drain-source channel. The maximum voltage on the primary winding of the transformer can be calculated to 84 V, but tests showed that the voltage at the primary winding and the transistor can exceed 150 V during faulty switching cycles. Accommodating an additional safety margin leads to a minimum drain-source voltage of 250 V for the transistor selection. The *ON* resistance of the drain-source channel is the major factor for power losses inside of the transistor. An *ON* resistance of 30mΩ combined with the maximum switching current and the calculated duty cycle leads to a power dissipation of 0.9678 W. Performed tests showed that the heat generated by this amount of dissipated power does not require additional measures for compensation.

The implemented design (see figure 3.16) features a low-side switch, therefore an N-channel Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFFT) has to be chosen.

The IRFB4332PbF by *International Rectifier* is a N-channel MOSFFT with a maximum drain-source voltage of 250 V and an *ON* resistance of 29 mΩ and was therefore chosen for the design [15].

Figure 3.18 shows the transformer with input- and output capacitors and diodes:

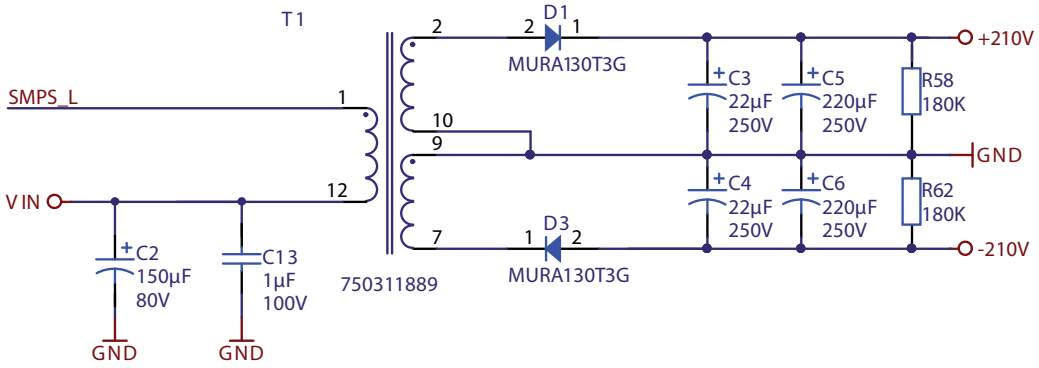

Figure 3.18.: High-voltage power supply transformer, input- and output capacitors and diodes.

It is recommended to choose input capacitors "in the range of 100 μF to 200 μF" [7, p. 24]. For the high-voltage power supply 150 μF are used as input capacitors. To minimize losses, in- and output capacitors should have minimal Equivalent Series Resistance (ESR) and Equivalent Series Inductivity (ESL) values. The *Panasonic FK* series brings this characteristics, contains a wide variation of capacitance and voltage combinations and has a good availability at common distributors of electronic components. Low ESL values are generally achieved by the usage of surface mount devices.

The output capacitor needs to handle the maximum *rms* current, which can be calculated according to equations 3.20 and 3.21 [7, p. 24]:

$$\Delta i_{\mathrm{L}} = \frac{D \cdot V_{\mathrm{in1}}}{2 \cdot L \cdot f} = 0.7613 \text{ A} \tag{3.20}$$

$$I_{\mathrm{COUT,RMS}} = \sqrt{(1-D) \cdot \left[I_{\mathrm{out}}^2 \cdot \frac{D}{(1-D)^2} + \frac{\Delta i_{\mathrm{L}}^2}{3} \right]} = 0.5565 \text{ A} \tag{3.21}$$

The output capacitors need to withstand 210 V, but the *Panasonic FK* series does not contain capacitors with these voltage ratings. Therefore, capacitors manufactured by *EPCOS (TDK)* from the *B43821* series which a voltage rating of 250 V and maximum saw-tooth current of 680 mA are used as output capacitors [16].

The rectifier diode at the transformer output has to sustain the reverse output voltage, be capable of forwarding the ripple current and should have fast switching and low leakage current characteristics for minimal losses at the transition between on and off cycles and a low forward voltage drop.

The ripple current can be calculated according to formula 3.22 [7, p. 23]:

$$I_{\text{diode,peak}} = \frac{I_{\text{out}}}{1-D} + \Delta i_{\text{L}}^2 = 1.9280 \text{ A} \tag{3.22}$$

The selected diode `MURA130T3G` (by *ON Semiconductor*) is designed to withstand 300-400 V reverse voltage and has a low forward voltage drop of 0.8 V, as well as a fast recovery time of 65 ns [17], but it is only rated at 1 A forward current which is below the calculated diode peak current (formula 3.22). The graphs in the datasheet, however, show that the specified forward current of 1 A is an average value and the diode is capable of handling peak currents in square wave form of up to about 2.1 A [17, p. 4, figure 9].

3.3.2 Flyback Step-Down Converter

The second power supply circuit needs to generate ±15 V and +5 V from an input voltage between 24 V and 70 V.

The `LM5017` is used as controller IC for this switch-mode power supply. It is a synchronous controller with internal switches. Synchronous controllers replace the diode typically required in switch-mode power supplies by another controlled switch (transistor). Therefore, a higher efficiency can be achieved. The `LM5017` has a maximum input voltage range from 7.5 V to 100 V, is capable to provide up to 600 mA and has an adjustable switching frequency of up to 1 Mhz [18].

Texas Instruments provides a reference design featuring a quad-output ±15 V, ±5 V flyback-buck-converter for the `LM5017` [19]. This design uses the *Würth Elektronik* `750313955` transformer with four secondary windings and fits exactly the given requirements in this project.

Figure 3.19 shows the external circuit for the `LM5017` controller IC as presented in the reference design by *Texas Instruments*:

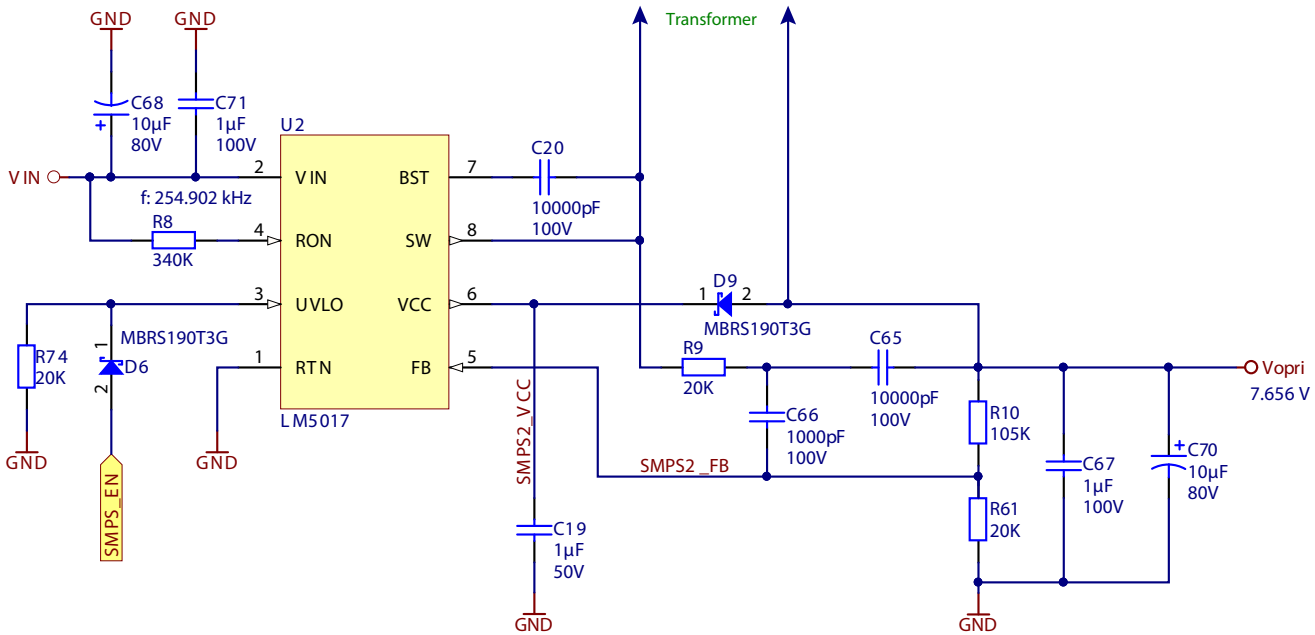

Figure 3.19.: Switch-mode power supply featuring the `LM5017` controller IC. [19]

The 340 kΩ resistor to the RON pin sets a switching frequency of 254.902 kHz. In contrast to the high-voltage switch-mode power supply, this circuit uses the voltage from the primary winding to regulate the output voltage. A primary side output voltage of 7.656 V yields output voltages of ±15.31 V and ±5.1 V. The voltage divider formed by resistors R10 (105 kΩ) and R61 (20 kΩ) gives a feedback voltage of 1.225 V which is equal to the internal reference voltage.

The output voltage at the primary side is also used as supply voltage for the controller IC itself, using diode D9.

The UVLO pin is used to provide control over the circuit to the microcontroller on the board and is designed exactly the same as in the high-voltage power supply circuit.

Figure 3.20 shows the transformer itself with the circuitry connected to the secondary windings:

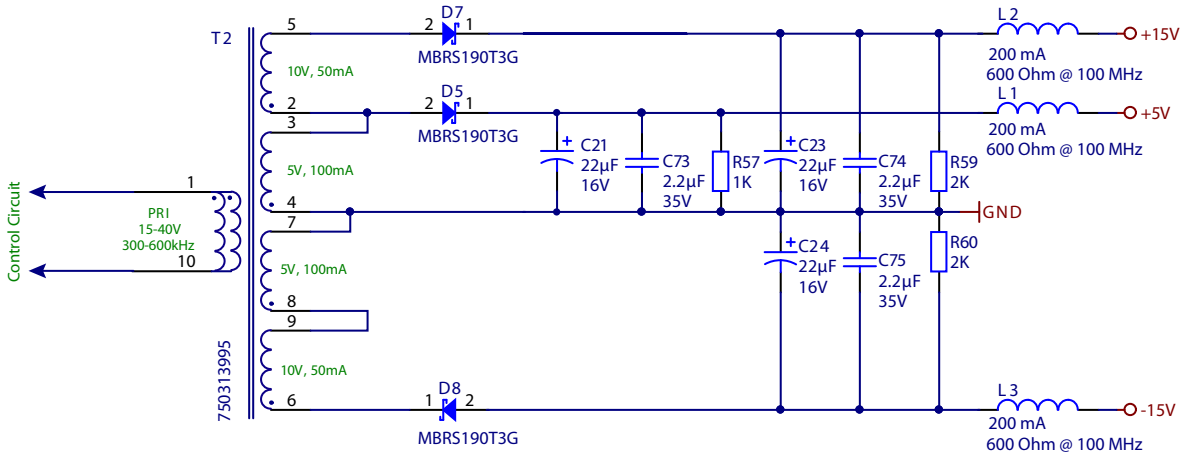

Figure 3.20.: WE 750313995 transformer with external circuitry.

The diode MBRS1100T3G (by *ON Semiconductors*) is used as diode on the secondary side. This diode has a nominal forward current of 1.0 A and can withstand 100 V reverse voltage. Being a *Schottky* diode it has a very short recovery time for high efficiency.

In contrast to the reference design, the −5 V output voltage is not required in this project and therefore the respective output from the transformer (pin 8-9) is not used. To increase the output voltage stability and reduce noise, additional 22 μF output capacitors and ferrite beads (L1 to L3) are used in this design.

3.4 Communication Interfaces

To provide means for communication between the controller and driver boards a respective interface has to be chosen and implemented on both sides.

Key characteristics for the communication interface are simple implementations on both sides in terms of required hardware components and effort required for the implementation of a communication protocol in the software. Another key characteristic is reliability and resilience in harsh environments with high-frequency electromagnetic noise or noise induced by the switch-mode power supplies on the same boards.

Most microcontrollers have dedicated hardware support for three common low-level communication interfaces with no or very low additional protocol overhead: Serial Peripheral Interface (SPI), Inter-Integrated Circuit (I^2C) and Universal Asynchronous Receiver Transmitter (UART).

SPI has no means for addressing different parties connected to the same bus implemented in the protocol, but requires a dedicated *slave-select* line for each receiver. Bus participants are also distinctly categorized in master (provides clock) and slave (responds to master) devices. [20]

I^2C allows multiple masters on the same bus and provides a standardized protocol for addressing receivers, which has a very low overhead. The clock rate is lower than for SPI interfaces and specified at 100 kHz (400 kHz in fast mode) [21].

UART is a serial communication interface with no dedicated clock line and full-duplex capability by providing dedicated receive and transmit lines. UART interfaces are not bound to a single specification regarding the physical properties of transmitted signals, but there are a number of different specifications and standards available and widely used. Connections to *Personal Computers* are usually made using the *RS232* interface specification using single-ended ±12 V signals, but interfaces can also be implemented for differential signal transmission as specified in the *RS485* standard [22].

The major advantage of using differential signals is that induced noise on the transmission line cancels out at the receiver. Therefore, RS485 is used as communication interface leveraging the integrated UART peripherals in the microcontrollers but requires an additional transceiver IC.

Figure 3.21 shows the RS485 transceiver circuit for the conversion between 3.3-V-logic-level UART signals facing the microcontroller and differential RS485 signals for board-to-board communication:

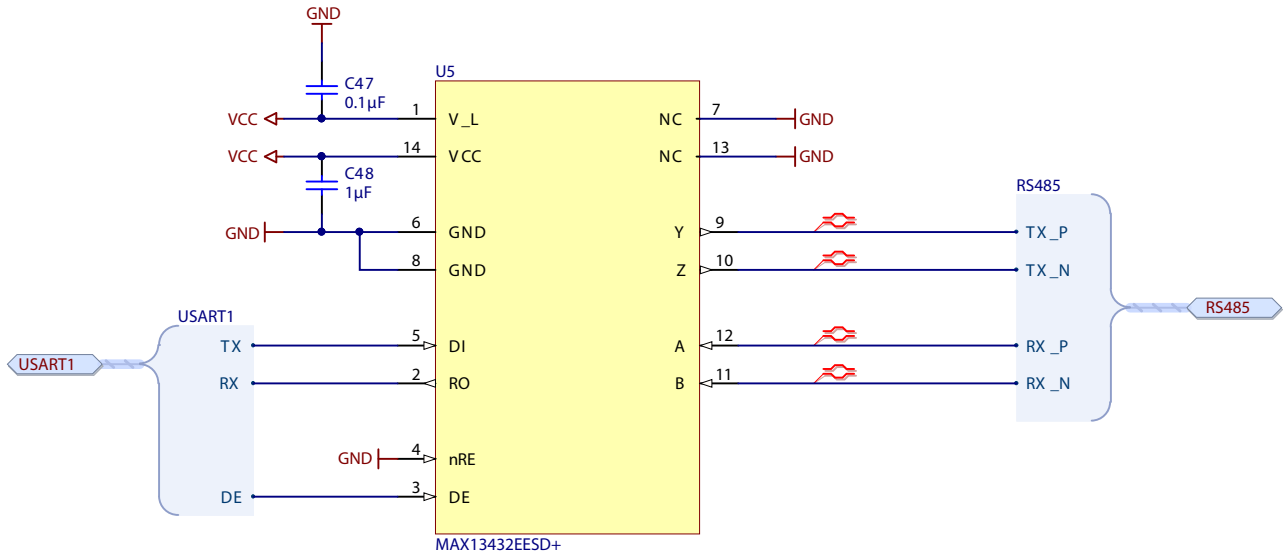

Figure 3.21.: RS485 transceiver with external circuitry.

The transceiver IC is a `MAX13432E` designed by *Maxim Integrated* supporting 500 kbps full-duplex operation and supply voltages down to +3 V [23]. The `VCC` pin (14) is equipped with a 1 μF by-pass capacitor for full ESD protection [23, p. 12]. The power supply pin for logic level signals (pin 1) is equipped with a 100 nF by-pass capacitor.

The fixed connection of the receive-enable (nRE) pin to ground ensures that the receiver sub-circuit is always enabled. To send data, the control circuit (microcontroller) has to enable the transmit sub-circuit by pulling the driver-enable (DE) pin to a high potential. When the transmit sub-circuit is not enabled differential output pins Y and Z are disabled and switched to high impedance mode. This enables other transceivers connected to the same bus to transmit data.

The driver board does not contain line termination resistors, because multiple driver boards can be chained together using the same *RS485* bus. Line termination on every board would increase the resistive load on the bus with every additionally connected driver board. Due to the low total line length of all connected *RS485* devices, termination for the differential lines is not necessary. If reflections on the transmission lines turn out to be an issue, dedicated plugs containing termination resistors could be used at the end of the chain of the driver boards to terminate the *RS485* transmission lines.

3.5 Control Circuit

The control block orchestrates the whole systems, receives control messages sent by the controller board and adjusts the system behavior accordingly. To do this it has to provide the following functionality:

1. Receive control messages from the controller board and send responses via UART.
2. Enable/Disable the (high-voltage) power supply blocks.
3. Generate the desired signal waveform (0 to 3.3 V) as an input to the operational amplifier circuit block and a 1.1 V offset voltage for balancing the waveform signal.
4. Set the resistor value of the digital potentiometer for gain adjustment of the operational amplifier via SPI.
5. Provide feedback to the user (Light Emitting Diodes (LEDs)) and take user inputs (buttons).
6. Capture the voltage output of the current sense amplifier.
7. Provide means for storing the configuration state of the system as start-up state to be loaded after power cycles.

The implementation of these versatile functions requires the usage of a microcontroller which can be programmed with a software for controlling the hardware on the driver board. The following figure gives an overview over the various functions implemented in the microcontroller and the dependencies to other components on the board:

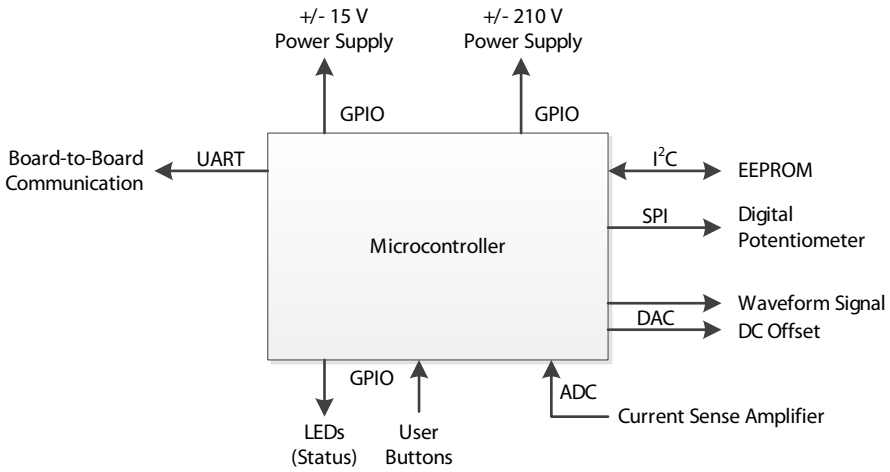

Figure 3.22.: Overview of the various functions implemented in the microcontroller.

The requirements to the microcontroller for implementing the described functions are not exceptional and any of the widely available 8-bit microcontrollers (e.g. *Atmel AVR®*, *Microchip PIC®*, etc.) could be used for the driver board, but the controller board has higher demands towards the microcontroller in both, regards of processing power, as well as connectivity options. Therefore a microcontroller with 32-bit ARM core is used in the driver board for being able to use a single toolchain for software development and allow easier software code reuse in both systems.

NXP and *STMicroelectronics* are two vendors offering a wide range of low-priced microcontrollers with *ARM Cortex-M* processing cores, but only *STMicroelectronics* offers microcontrollers with two DAC channels in their low pin count. Therefore, a `STM32F072CBT` is used as microcontroller in the driver board design. It is an ARM-based 32-bit microcontroller with 128 KB flash memory, 16 KB Random Access Memory (RAM), 12 timers, ADC, DAC with two channels, UART, I^2C and SPI communication interfaces [24].

The minimum required external circuit for the microcontroller is described in an application note [25] by *STMicroelectronics*. To prevent current spikes caused by synchronous switching of the internal microcontroller circuitry to propagate on the supply voltage rails through the board design, every power supply pin is equipped with a 100 nF decoupling capacitor. A 1 μF ceramic and a 10 μF tantalum capacitor provide further decoupling of the digital system centered around the microcontroller against the other components, connected to the 3.3 V *VCC* supply voltage.

The power supply for the analog sub-system of the microcontroller is connected by using separate pins of the IC. The analog supply voltage is decoupled from the power supply rails connected to the digital systems using a ferrite bead. A 100 nF ceramic and a 10 μF tantalum capacitor provide further decoupling for the analog circuitry of the microcontroller. The ground pin of the analog sub-system is connected to a separate analog ground net (`AGND`), which connects all analog systems on the board and is connected to the digital system ground at a single point on the board.

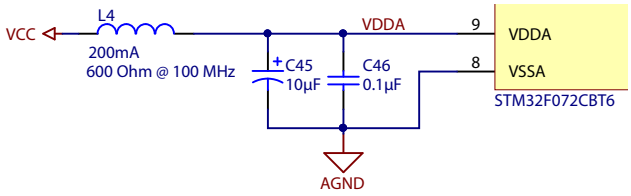

Figure 3.23.: Decoupling of the analog supply voltage for the microcontroller.

The microcontroller can be operated without external clock or crystal-oscillator circuits, but the accuracy of the internal oscillator is limited [25, p. 18] and external crystals can be implemented with little effort and at low costs. The microcontroller has the option to connect two external independent oscillators or crystals: a high speed external oscillator or crystal in the range between 4 MHz and 32 MHz for system clock generation and a low speed external oscillator or crystal with 32.768 kHz for accurate real time applications.

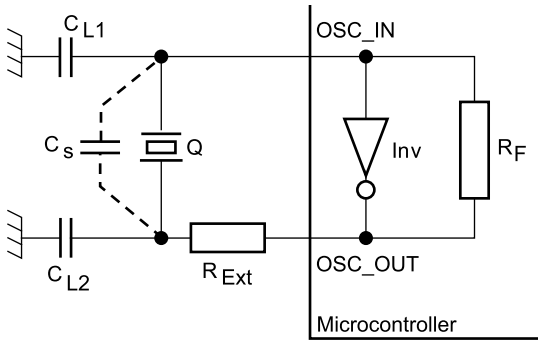

Figure 3.24.: Pierce oscillator design [26, figure 5, p. 11].

Providing external clock sources using crystals requires two additional resonate capacitors to form a *Pierce oscillator design* (figure 3.24) [26]. The value of these capacitors can be calculated by using the following equation containing the load capacitance (C_L) specified by the crystal manufacturer, an assumed capacitance of the signal traces and microcontroller pins (C_S) and the external load capacitances itself (C_{L1} and C_{L2}):

$$C_L = \frac{C_{L1} \cdot C_{L2}}{C_{L1} + C_{L2}} + C_S \tag{3.23}$$

The capacitance of the signal traces and microcontroller pins (C_S) can be estimated to around 5-10 pF [26]. The recommended load capacitance of the crystal used in this design is 20 pF. Therefore, the value for the external load capacitors for the high speed oscillator design can be calculated to 25 pF:

$$C_L - C_S = \frac{C_{L1} \cdot C_{L2}}{C_{L1} + C_{L2}} = \frac{C_{L1,2}}{2} \quad \Rightarrow \quad C_{L1,2} = 2 \cdot (20\ \text{pF} - 7.5\ \text{pF}) = 25\ \text{pF} \tag{3.24}$$

The design uses ceramic capacitors with 27 pF, being a standard capacitor value and still in the boundaries of the accuracy of the calculation, given that the capacitance of board traces and IC pins can only be estimated.

The circuit for the external high speed oscillator incorporates an additional 150 Ω resistance "to limit the drive level of the crystal" [26, p. 16]. It forms a low-pass filter with C_{L2} "that forces the oscillator to start at the fundamental frequency and not at overtones" [26, p. 16].

Figure 3.25 shows the external oscillator crystals with support circuitry connected to the microcontroller. The calculation of load capacitor values for the low speed external crystal is performed like for the high speed crystal (equation 3.23), except that the recommended total load capacitance, specified by

the manufacturer, is different and the low frequency oscillation does not require an external overdrive resistor.

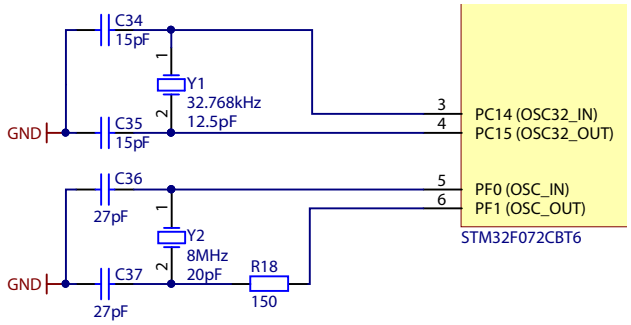

Figure 3.25.: External oscillator crystals with support circuitry connected to the microcontroller.

Microcontrollers of the `STM32F0xx` device family have three different boot modes, which can be selected by an external pin (`BOOT0`) and a boot select bit in the *user option byte* [25, p. 20]. Depending on the value of the boot select bit and the voltage level at the external pin, the microcontroller starts program execution from the main flash memory, the system memory or the embedded RAM. Main flash memory is the location of the custom firmware loaded into the microcontroller. The system memory section in the flash contains a bootloader and allows recovery when no valid firmware is loaded into the main flash memory section. Booting to RAM can be used by an externally connected debugger by setting the boot select bit in the *user option byte*.

Table 3.1 shows the selected boot mode, depending on the value of the boot select bit `nBOOT1` in the *user option byte* and the voltage level at the `BOOT0` pin.

Table 3.1.: Boot modes of microcontrollers in the `STM32F0xx` family.

nBOOT 1 bit	BOOT0 pin	Mode
x	0	Main Flash memory
1	1	System memory
0	1	Embedded RAM

The `BOOT0` pin can be connected to 3.3 V or ground using a 3-position jumper on the driver board. A 4.7 kΩ resistor limits the current to the pin and acts as a simple low-pass filter to reduce the influence of noise present on the ground or 3.3 V signal planes.

Debug connections to microcontrollers are traditionally implemented using the JTAG protocol and the respective universal interface specification (IEEE1149.1), but the `STM32F072` is designed with low pin count and does not implement a JTAG interface. Connections for debugging the running firmware and supplying new firmware to the internal flash of the `STM32F072` can be accomplished using the *ARM* Serial Wire Debug (SWD) protocol and interface. SWD uses a single clock and data line for this purpose. The connection between a programmer/debugger and the board can be made by using a 10-pin connector with the pin-out designed according to the recommended standard [25, figure 9, p. 23]. Figure 3.26 shows the connector pinout implemented on the board:

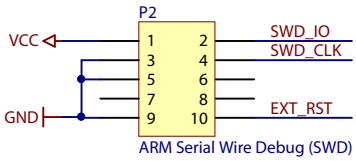

Figure 3.26.: Serial Wire Debug (SWD) connector on the driver board.

The SWD connector also contains a reset line which is connected to the respective pin of the microcontroller. A microcontroller reset can also be triggered by a button on the board. A 10 nF capacitor and a 1 kΩ resistor placed close to the microcontroller form a low-pass filter to protect the reset pin of the microcontroller from external noise induced on the line, and prevent the microcontroller from entering the reset state erroneously. A 10 kΩ pull-up resistor assures a safe default state of the reset line. The described circuitry is shown in figure 3.27:

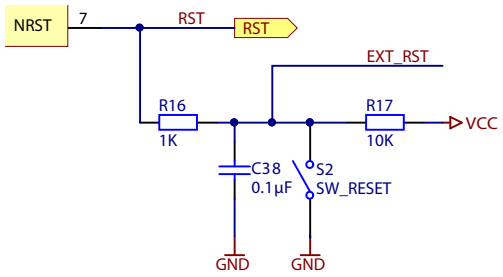

Figure 3.27.: Reset connections and noise filtering at the microcontroller.

The (filtered) reset signal is also connected to the digital potentiometer IC. A reset of this IC sets the resistor value to the default center position. Further connections between the microcontroller and the digital potentiometer include the default SPI lines (*clock*, *data in*, *data out* and *slave select*) and a dedicated *ready* signal, which is driven by the digital potentiometer to signal completed configuration write operations to the microcontroller.

The output of the current sense amplifier is connected to an ADC pin of the microcontroller. The current sense amplifier has a 5 V power supply, but the ADC pins of the `STM32F0xx` microcontrollers must only be connected to signals with a voltage range between 0 V and `VDDA` (3.6 V maximum, 3.3 V in practice) [24]. Therefore a 3.3 V *Zener diode* is added to protect the pin from higher voltages. An additional 20 Ω resistor limits the current through the *Zener diode* to a maximum of

$$\frac{5\ \text{V} - 3.3\ \text{V}}{20\ \Omega} = 85\ \text{mA}. \tag{3.25}$$

Figure 3.28 shows the described overvoltage protection circuit of the ADC input pin of the microcontroller:

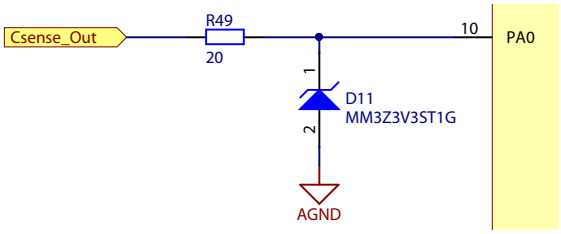

Figure 3.28.: Overvoltage protection of the ADC input pin of the microcontroller.

Both DAC output channels of the microcontroller are used to generate the desired waveform signals. One DAC channel generates the actual waveform with a voltage range from 0 V to 3.3 V, while the other supplies a switchable offset voltage of 1.1 V, required for balancing the DAC signal around 0 V by the first operational amplifier stage (see section 3.1.1). The DAC has a maximum operating frequency of 1 MHz and a typical settling time of full-scale output changes of 3 μs [24, table 61, p. 90]. Tests with a first prototype implementation of the board showed that the signal generated by the DAC contained high frequency noise components. Therefore the DAC output channel which provides the waveform signals contains an additional passive low-pass filter, build from a 100 Ω resistor and 4.7 nF capacitor leading to a cutoff frequency of about 340 kHz.

The internal state of the system is signaled to the user through five LEDs. A `TX` and a `RX` LED signal transmit and receive operations of the UART. A `BLINK` LED blinks with a fixed rate driven by the firmware main loop to signal continuous operation of the system. An `ACT` LED signals the state of the *arbitrary waveform generator* (on or off). The `PWR` LED signals the state of the power supply circuit blocks (on or off). All LEDs are connected to `VCC` using a 180 Ω resistor. This limits the forward current to less than 10 mA[1]. The cathode of the LEDs is connected to a dedicated microcontroller pin.

A single button is included on the board to allow direct interaction of a user with the firmware on the microcontroller beside control through the connection to a computer. The button connection to the microcontroller contains a 100 nF filter capacitor and a 10 kΩ pull-up resistor assuring a defined default state.

The `STM32F072` microcontroller does not contain a non-volatile data memory to save a configuration as start-up state to be applied after power cycles. Therefore, an external 16 kbit *EEPROM* is part of the control circuit as a separate component. The EEPROM IC is a `24AA16` by *Microchip* which is controlled using a I^2C connection [27]. The I^2C connections to the microcontroller are connected to a 4.7 kΩ pull-up resistor each, which is in the valid pull-up resistor range as specified in the standard document [21, p. 55]. The IC has a write-protect pin (`WP`) which is not used in the design and therefore connected to 0 V (ground).

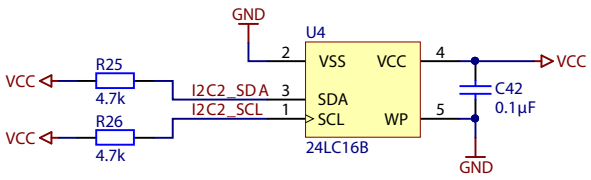

Figure 3.29.: EEPROM component with support circuitry.

[1] Figure 2, "Forward Current vs. Forward Voltage" `http://media.digikey.com/pdf/Data%20Sheets/Lite-On%20PDFs/LTST-C170GKT.pdf`

Different revisions of the hardware design of the driver board might require different behavior of the firmware deployed on the microcontroller. To provide means for the firmware to adapt to the hardware version it is running on top of, a 3-bit hardware version can be set by using resistors (see figure 3.30). The chosen implementation of this feature using resistors which placement can be changed, allows PCB layout independent adaption of the hardware version to manual changes or extensions of the hardware.

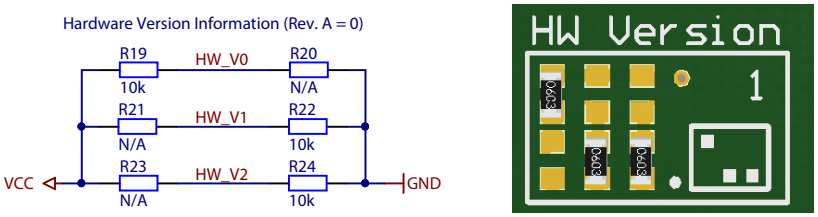

Figure 3.30.: Hardware version setting with schematic (left) and example layout (right).

3.6 Controller Board

The previous sections described design and functionality of the driver board, which implements all the major requirements of the project. Controlling this driver board requires an additional board with a *USB* connection to a computer and multiple RS485/UART connections to the connected driver boards. The controller board also contains the power supply circuit for the 3.3 V supply voltage of all boards (see section 3.3).

3.6.1 Power Supply

The power supply on the controller board has to generate a constant 3.3 V supply voltage for the digital circuitry of the controller board itself and all connected driver boards. The input voltage range is the same as for the driver board, which is 24 V to 70 V. For the presented 4-by-4 channel design 16 driver boards can be connected to a single controller board. Therefore the power supply circuit on the driver board has to be designed to supply current to 16 driver boards and its own digital circuitry. Measurements of a driver board prototype showed that the current consumed by a single driver board is always less than 50 mA. This leads to a maximum current of 800 mA required for the maximum supported number of driver boards. The goal for the power supply on the controller board was therefore to provide a maximum current of 1 A to include a safety margin for additional, extraordinary current demands.

The power supply on the controller board is implemented as switch-mode power supply in step-down configuration using the `MAX5035AASA+` controller IC by *Maxim Integrated*. The `MAX5035` is a 1 A, 76 V, high-efficiency (i.e. synchronous) step-down DC-DC converter [28]. The first character after the model number denotes the nominal output voltage of the DC-DC converter. The utilized `MAX5035AASA+` has a nominal output voltage of 3.3 V, which can be directly connected to the feedback pin of the IC without the requirement of a voltage divider feedback network.

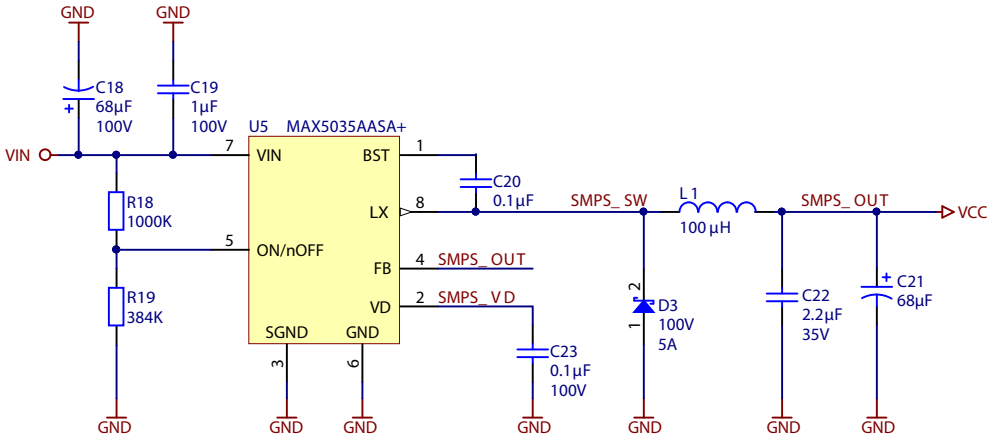

Figure 3.31.: 3.3 V switch-mode power supply.

The supporting circuitry (figure 3.31) for the `MAX5035AASA+` is used as specified in the datasheet [28, figure 2, p. 13]. Changes compared to the given reference circuit are an additional 1 μF capacitor at the `VIN` pin, an additional 2.2 μF capacitor at the output and a `PDS5100-13` 5 A, 100 V diode by *Diodes Incorporated* in `POWERDI5` package instead of the though-hole mounted diode used in the reference design.

The `MAX5035` includes an under-voltage-lock-out functionality to cease operation when the input voltage is under a certain threshold. This is accomplished by the voltage divider connected to the `ON/nOFF` pin of the IC. The threshold voltage of this pin is 1.69 V with 100 mV hysteresis [28, p. 10]. Resistors R_{18} (1000 kΩ) and R_{19} (384 kΩ) set the threshold for the input voltage to 6.6677 V. This is slightly above the minimum recommended input voltage of 6.5 V for an output voltage of 3.3 V as specified in the datasheet [28, p. 10]. *Maxim Integrated* recommends using the `MBRM5100` by *Diodes Incorporated* (surface-mounted) or the `50SQ100` by *International Rectifiers* (through-hole mounted) diodes as rectifier diode. The `MBRM5100` by *Diodes Incorporated* is no longer available and therefore replaced in this design by the recommended successor `PDS5100`.

3.6.2 Input Protection

The circuits on the controller and driver boards could come to considerable damage, if the external power supply was connected with reverse polarity to the inputs of the controller board. Therefore, a small protection circuit is required to protect the components on the board from damages, caused by powering the system with reversed polarity.

A simple solution to protect the circuits from reverse polarity is implementing a half- or full-bridge rectifier build from two or four diodes. This approach leads to a constant voltage drop for the input voltage and also incorporates a slightly shifted ground potential compared to the connected DC power supply. The constant voltage drop at the diodes results in an increased power dissipation of the system. Typical diodes with sustained reverse voltages of about 100 V and a few ampere current rating have a forward voltage drop of about 0.7 V to 1 V. To improve this circuit the same approach as used in synchronous DC-DC converts can be applied: diodes are replaced by MOSFFTs, which are switched on exactly when the diodes would be in forward-active mode [29].

This approach, shown in figure 3.32, uses the voltage difference between `VIN` and ground (`GND`) to switch the P-channel MOSFFT. A P-channel MOSFFT has a negative internal threshold voltage, therefore the

MOSFFT does not switch on when the GND potential is above the potential at VIN. This is the correct behavior when the voltage connected to the input terminals of the system is in reverse polarization.

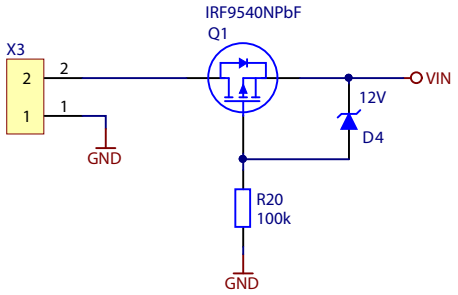

Figure 3.32.: Reverse polarization input protection circuit.

The MOSFFT in this circuit switches on when the gate potential is below the potential at the source pin, with a voltage difference being greater or equal to the threshold voltage (V_{th}) of the MOSFFT. When a voltage is applied to the input terminals with correct polarization the gate terminal is at ground potential of the connected power supply. The drain terminal is at the voltage potential of the connected input voltage. Therefore the diode incorporated in the MOSFFT between the drain and source terminal is in forward-active mode and the potential of the source terminal is at $V_{\text{in}} - V_{\text{forward, diode}}$. This leads to a voltage difference between the source terminal and the gate terminal greater than the internal threshold voltage for relevant input voltages (above 1 to 2 V). Therefore the MOSFFT switches on and the drain and source terminals are at roughly the same voltage potential. At this point the voltage drop between drain and source terminals, and therefore the dissipated power in the MOSFFT, is determined by the internal *on resistance* of the MOSFFT and the current drawn by the system. To minimize the dissipated power a P-channel MOSFFT with low *on resistance* has to be selected. The used P-channel MOSFFT `IRF6540NPbf` by *Internal Rectifier* has a specified *on resistance* of 0.117 Ω [15].

The maximum gate-source voltage of the used MOSFFT is specified at ±20 V [15]. This is less than the maximum input voltage of the system, being $+70V$. A 12 V *Zener* diode is therefore placed between the gate and source terminals of the MOSFFT to limit the source-gate voltage to a maximum of 12 V. When the supplied input voltage is above this 12 V limit, the resistor R_{20} limits the current through the *Zener* diode to a maximum of

$$\frac{V_{\text{in}} - V_{\text{zener}}}{R_{20}} = \frac{70\ \text{V} - 12\ \text{V}}{100\ \text{k}\Omega} = 0.58\ \text{mA}. \tag{3.26}$$

3.6.3 Microcontroller

Central component on the controller board is the microcontroller. This microcontroller should be in the same series as the microcontroller on the driver board (`STM32F072`) to enable an homogeneous development environment for the software of both boards, have four simultaneously usable UART interfaces, a Universal Serial Bus (USB) device interface and enough RAM to be able to manage connections to up to 16 connected driver boards. The selected `STM32F103RG` meets these requirements. It has 1 MB flash memory, 96 KB RAM, 5 UARTs, an USB device interface and can be clocked with a frequency of up to 72 MHz [30].

The general support circuitry for the microcontroller is implemented exactly identical as for the microcontroller on the driver board (see section 3.5). This includes power supply decoupling, oscillators, debug interface and buttons. The controller board has two LEDs: a blink/alive LED indicating general system health and an additional LED to be used by software to indicate internal states. The controller board contains the same circuit for setting the hardware version as the driver board.

The controller board also contains an external EEPROM as non-volatile memory. The IC is the same as on the driver board and the supporting circuitry is described in the respective section (see also figure 3.29).

Microcontrollers of the `STM32F1xx` family have three different boot modes, which can be selected by two external pins (`BOOT0` and `BOOT1`) [31, p. 15]. Depending on the voltage levels at the external pins, the microcontroller starts program execution from the main flash memory, the system memory or the embedded RAM. The main flash memory is the location of the custom firmware loaded into the microcontroller. The system memory section in the flash contains a bootloader and allows recovery when no valid firmware is loaded into the main flash memory section. Booting to RAM can be used to reset the microcontroller while still keeping the (temporarily) loaded firmware in the RAM.

Table 3.2 shows the selected boot mode depending on the voltage levels at the `BOOT0` and `BOOT1` pins.

Table 3.2.: Boot modes of microcontrollers in the `STM32F1xx` family.

BOOT1 pin	BOOT0 pin	Mode
x	0	Main Flash memory
0	1	System memory
1	1	Embedded RAM

The `BOOT0` pin can be connected to 3.3 V or ground by using a 3-position jumper on the controller board. A 4.7 kΩ resistor limits the current to the pin and acts as a simple low-pass filter to reduce the influence of noise, present on the ground or 3.3 V signal planes. The `BOOT1` pin is already connected to the *drive enable* pin of the RS485 transceiver of the second communication channel (`UART2_DE`) and therefore tied to ground using a 10 kΩ pull-down resistor (see section 3.6.4).

3.6.4 Communication Channels

Main purpose of the controller board is to act as communication hub between an USB connection to a computer and the four RS485 communication channels to connected driver boards.

Figure 3.33.: The communication channels on the controller board.

The connections between driver boards and the controller board are made by using the differential RS485 standard (see section 3.4). The `MAX13432E` by *Maxim Integrated* is used as transceiver IC to transform the logic level UART signals from the microcontroller to differential signals, as defined in the RS485 standard.

The only difference to the circuit implemented on the driver boards are the 120 Ω termination resistors (R_{16} and R_{17}) on the differential lines. The controller board is always the last device in the chain and can therefore contain termination resistors to reduce reflections on the bus.

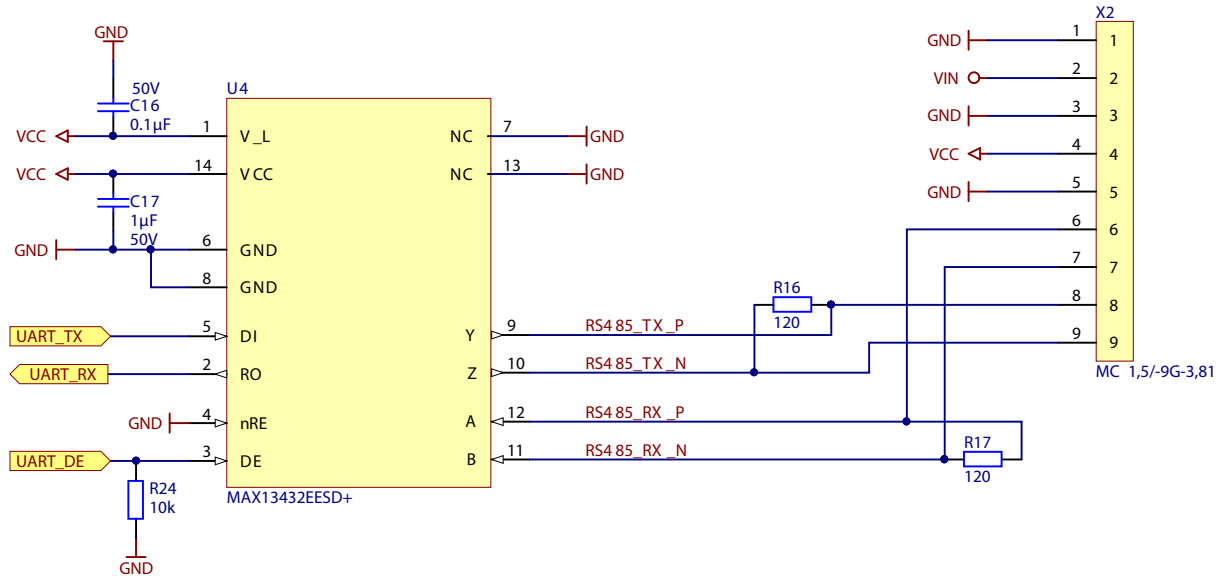

Figure 3.34.: RS485 transceiver connecting the controller board to a driver board.

The RS485 transceiver circuit is implemented four times, as shown in figure 3.34, for the four communication channels to the driver boards.

Communication on the RS485 bus has to happen between a single controller board and one or multiple connected driver boards. Therefore, all driver boards use the same differential pair of lines for sending data and the other differential pair for receiving data. The controller receives data on the differential pair connected to the transmitters on the driver boards and sends data on the differential pair connected to the receivers on the driver boards. This bus structure allows full-duplex communication on the bus.

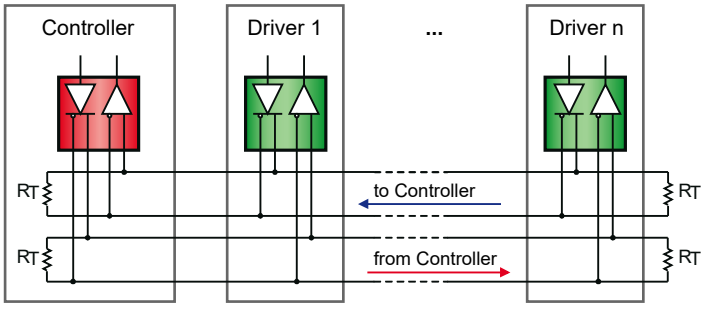

Figure 3.35.: Structure of the RS485 bus connecting the controller board to multiple driver boards.

Implementing the bus in full-duplex mode as shown in figure 3.35 implies that collisions can occur when multiple driver boards send data at the same time. Due to the full-duplex implementation, senders can not determine collisions by themselves, because they can not sense the line connected to their transmitter. Therefore the protocol used for communication between the boards needs to provide measures to detect collisions on the bus. No collisions can occur when the controller board sends data, because it is the only sender on the respective differential pair of lines.

Universal Serial Bus (USB)

The connection to a computer controlling the system uses an USB interface. The microcontroller on the controller board incorporates an USB interface following the USB 1.0 *Full Speed* standard with a connection speed of 12 Mbit/s [30, p. 22]. To indicate a connected device supporting *Full Speed* connections, the `D+` line of the USB interface has to be connected to the 3.3 V supply voltage by using a 1.5 kΩ pull-up resistor (R_{23} in figure 3.36).

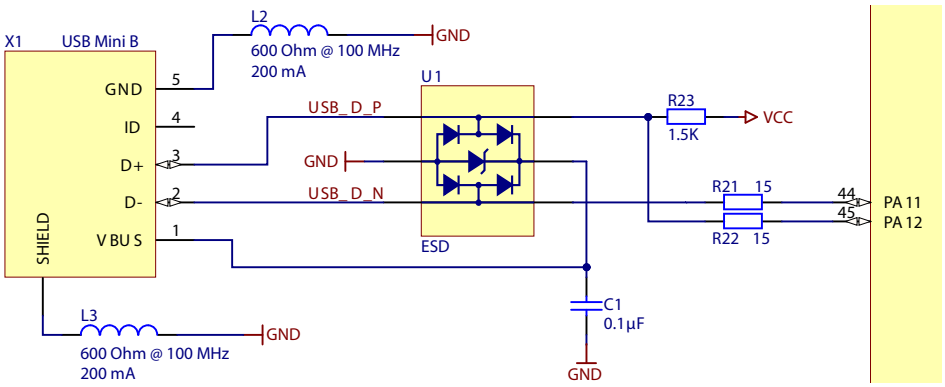

Figure 3.36.: USB interface circuit on the controller board.

To protect the controller board from hazardous high voltages the `USBLC6-2` ESD protection circuit (by *STMicroelectronics*) is used to shortcut voltages on the data lines of the USB interface outside the allowed voltage range to the ground (`GND`) or `VBUS` supply voltage rails. Pins `PA11` and `PA12`, which are used for the USB interface on the microcontroller, are 5 V tolerant [30, p. 33].

Ferrite beads between the ground and shield connections of the USB connector and the ground planes of the controller board provide shielding against high frequency noise from a connected USB cable. High frequency noise on the data lines of the USB interface is reduced by 15 Ω series resistors right next to the respective microcontroller pins.

4 Implementation

The previous chapter describes the design of the circuit blocks composing the high-voltage signal generator system and discusses design decisions made leading to the final version of the system. To get from this system description in schematic from to a final design for manufacturing, the design has to be transformed into a layout which is the blueprint for PCB production.

4.1 General Considerations

The following sections discuss general considerations and design decisions taken into account for the implementation of the design before going into detail discussing the distinct sections of the system and their layout.

4.1.1 Component Selection

The foregoing *Design* chapter discusses the system design and selection of key ICs in detail. For passive components only the characteristical value of the component is discussed and included in the schematic. Finishing the design for manufacturing requires the selection of distinct products for the passive components as done for the ICs. The following section discusses the considerations taken into account for selecting these components. A detailed listing of all components is included in the appendix (section B.4).

Surface mounted (SMD) components are selected when ever possible to minimize the required space and simplify automated placement of components on the PCB. Standard size of the used SMD components is `0805`, larger sizes are selected when higher current or voltage ratings are required. SMD component sizes down to `0603` are used for areas on the PCB with high component density.

For all resistors three characteristics are taken into account in the selection of suitable components: the resistor value, the maximum voltage across the terminals and the maximum current though the resistor. When current and voltage requirements for a resistor are not static, maximum values are taken from *SPICE* simulations performed for all major designed circuits. All resistors have a tolerance rating of 1 %. Components from the `MCR` series by *Rohm Semiconductor* are used as standard resistors when no special requirements for voltage or current are given. Resistors from the `MCR` series are rated up to 150 V (for the `0805` size). Resistors for the high-voltage sections of the design are chosen from the `KTR` series by *Rohm Semiconductor*. They are rated at 400 V (for the `0805` size). Resistors dissipating a large amount of power are chosen from various manufacturers as suitable.

For the selection of suitable capacitors the maximum voltage present across the terminals is critical to prevent damaging the capacitors. Ceramic capacitors are used in the design in three voltage categories: 50 V, 100 V and 250 V. Ceramic capacitors are available with even finer distinction in terms of the rated voltage, but limiting the categories to these three voltages allows reuse of component types and therefore greater order quantities leading to a reduced price per component.

4.1.2 PCB Design Rules

The PCB is manufactured by *Würth Elektronik*, therefore their published PCB design rules define the base line for the design rules used in this project. Key elements of these design rules are the minimum track width (150 μm), spacing (150 μm), drill diameter (0.25 mm), and pad size for vias, etc. (0.60 mm) [32].

The second defining factor for the design rules is the voltage of the respective signal traces. The *IPC – Association Connecting Electronics Industries* published the IPC-2221A standard which specifies, amongst other figures, the minimum spacing requirements for different voltage levels in electronic systems. The spacing rules defined in the standard document are grouped in categories referencing the context for the spacing rules. The category `B1` is used for "internal conductors" like PCB traces [33, p. 42]. Table 6-1 *Electrical Conductor Spacing* defines for the `B1` category a minimum spacing requirement of 200 μm for voltages in the range between 171-250 V. For voltages ranging between 301 and 500 V, a minimum spacing requirement of 250 μm is defined [33, table 6-1, p. 43]. Voltages on the traces belonging to the the high-voltage part of the system range between -210 V and $+210$ V. The minimum spacing requirement for these traces is set to 300 μm to incorporate an additional safety margin. The minimum spacing (clearance) for other signals in the system is set to the minimum required spacing by the PCB manufacturer: 150 μm.

A complete report of the design rules is included in the digital media delivered with this thesis for full inspection.

4.1.3 Connectors

Connections between the driver boards and the driver and controller board are made using a single cable including power and data signals. The current rating of the connector has to be suitable for powering four driver boards connected in series. Therefore, a 9-pin socket connector from the `MC-1,5` series by *Phoenix Contact* with 3.81 mm pitch is chosen for linking driver and controller boards. It has a current rating of 8 A and voltage rating of 160 V. The matching plug to the connector has screw terminals eliminating the need for special crimp tools leading to reduced total manufacturing costs.

Table 4.1 shows the pin assignment of the connector. `TX/RX` pins are labeled as seen from a driver board. The pin assignment of the sockets is also included on the silkscreen on driver and controller boards for convenience.

Table 4.1.: Pin assignment of connector linking driver and controller boards.

Pin	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
Function	Ground	VIN	Ground	3.3 V	Ground	TX+	TX-	RX+	RX-

The output connectors on the driver board are implemented using a two terminal connector from the `MC-1,5` series by *Phoenix Contact* with 5.08 mm pitch for higher voltage sustainability and the ability to have a fully assembled, removable plug for quick changes of the connected load. A two position screw terminal by *Phoenix Contact* is added as second option to provide greater flexibility for the end user.

Power to the controller board can be provided using standard 4 mm *banana* connectors being commonly used in lab environments. Two color-coded (black and red), vertical sockets manufactured by *Deltron Components* are included on the controller board for this purpose. Additionally a two terminal connector

from the MC-1,5 series by *Phoenix Contact* in featured on the board which can be used for powering the system as well.

4.1.4 Manufacturing

Manual assembly of the PCB is facilitated by including designators for all active and passive components on the silkscreen on the top and bottom side of the PCBs. Placement of components with distinct polarity is eased by additional dot and line symbols on the silkscreen providing information of the correct polarity for all relevant components.

PCB assembly using automated *pick-and-place* tools is supported through the placement of three fiducials on the top and bottom side of the PCBs. The fiducials allow automated control of the PCB position and orientation and respective tool calibration for correct placement of components. Fiducials are created following the industry standard with a 0.040 inch round pad and a 0.100 inch soldermask clearance [34, 2.5.8, p. 20]. No components or traces must cross or overlap the 0.100 inch clearance to ensure best possible recognition of the fiducials and maximum contrast for digital imaging systems incorporated in the *pick-and-place* tools.

4.1.5 Mechanical

The driver board is equipped with six holes to screw the board into a housing for better handling. The holes have a diameter of 3.3 mm allowing the usage of standard M3 screws. Mechanical stability of the copper layer connecting the screws to ground potential is fostered by six vias distributed around the screw hole with an equal spacing of 60°.

The controller board is equipped with four screw holes, designed according to the previous description.

4.2 Driver Board

The layout of the driver board contains analog, as well as digital circuitry, generates high-voltages, and can be chained with further driver boards. These properties have to be taken into account for the physical layout of the board. Noise generated by high frequency switching digital circuits should not be induced to analog traces, the same is true for connections from the input to the output connector for chaining driver boards. The influence of any electrical effects produced by connected boards should not influence the operation on a driver board providing the connection to further boards. For the high-voltage circuit blocks it has to be made sure, that the effect of failing components in these blocks is minimal to components on the other circuit blocks. Furthermore, it is required to inform the user which parts of the PCB contain high-voltages and must not be touched when manually interfering with the system on the board.

Figure 4.1 shows the division of the driver board into many distinct blocks. The red line in the figure separates the high-voltage part (right side) from the logic level circuit blocks. The presence of high-voltage on the right part is signaled to users by clearly visible warning signs and imprints on the silkscreen. The section containing high-voltages is also separated by a continuous white line on the silkscreen. The only traces crossing these two sections are ground and input voltage traces at the top of the displayed board graphic in figure 4.1. All other connections between these two sections are made using components (resistors, capacitors and diodes) bridging and suitable to sustain the high voltage difference.

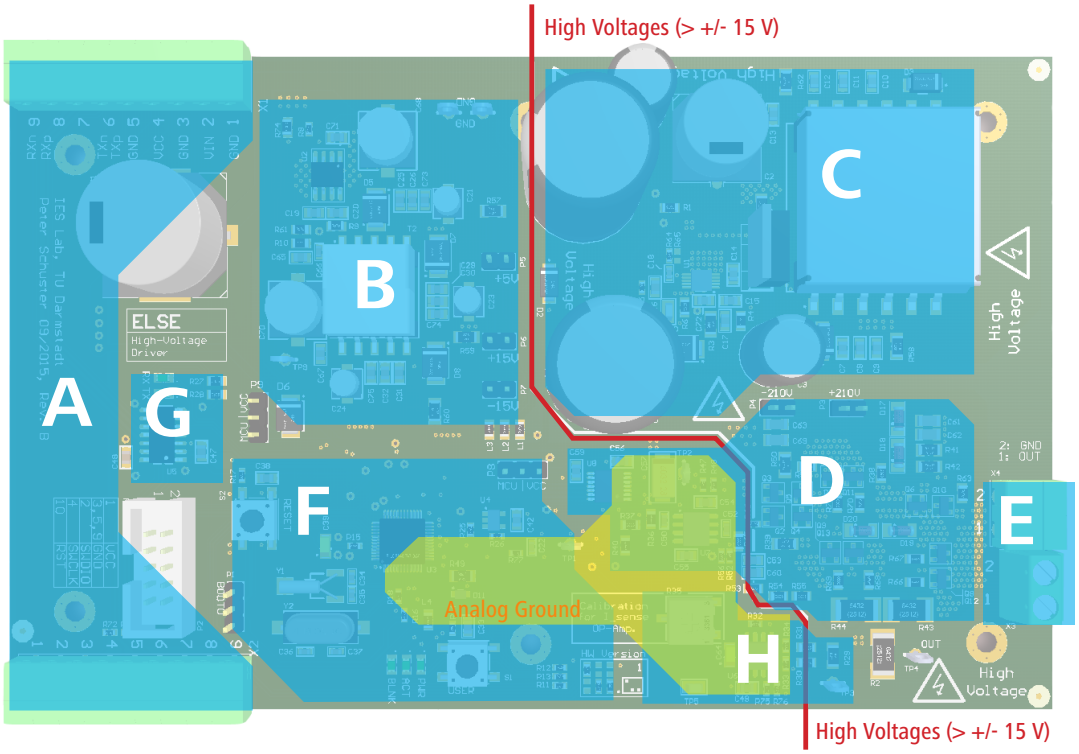

Figure 4.1.: Placement of circuit building blocks on the driver board.

On the left side of the driver board are the *input* (top) and *output* terminals to connect another driver board to the same communication channel of the controller board. All power connections between the two connectors are made with thick traces for minimum impedance on the left side of the board (section **A**). The RS485 transceiver is placed in section **G**, tapping the communication lines between both connectors on the board.

The step-down DC-DC converter for ±15 V and +5 V is placed in section **B** for maximum distance to analog circuitry, but in line between the input connector and other circuits giving a good central connection point for ground return currents of the generated voltages. The high-voltage step-up DC-DC converter is placed in section **C** which is in the high-voltage part of the PCB and also has the greatest distance to analog signals. Especially the transformer is placed in the corner of the PCB for this reason.

The operational amplifier block generating the high-voltage output signal from logic level inputs is placed in section **D**. It is mostly part of the high-voltage section on the PCB, but also contains components with lower supply voltage on the left side of the high-voltage division line. The output connectors providing access to the generated signal are placed in section **E** at the right side of the PCB. The current sense amplifier is placed in section **H** being close to the generated output of the system while keeping great distance to the noisy DC-DC converters. The block contains high, as well as low voltages and must therefore be placed at the intersection of the high- and low-voltage sections.

The digital control circuit is placed in section **F**. It has connections to almost all other sections and controls the operation of the system. The analog part of the control circuit, as well as the current sense amplifier and the operational amplifiers are placed on a separate analog ground plane (yellow section in figure 4.1). No high frequency digital signals are routed through this area on the PCB. The analog ground plane is connected at a single point between sections **B** and **F** to the remaining ground plane. This ensures that no return currents originated in digital circuits crosses the analog ground plane. The

single connection between sections **B** and **F** is placed at this point to ensure that supply voltage currents (originated in section **B**) and corresponding return currents on the ground plane do not form a loop. Therefore electromagnetic fields generated by the currents cancel each other out not influencing other circuits.

The outputs of the switch-mode power supplies to the other sections on the board are connected using two-pole jumpers. Therefore the sections can be assembled and tested separately. The jumpers also allow injection of test signals as input to following sections.

Beside these general considerations involved in the layout of the driver board, the layout of each of the sections involved different challenges discussed in the following sections.

4.2.1 Layout of the Step-Down Switch-Mode Power Supply

Three key constraints have to be considered when designing the layout of switch-mode power supplies:

1. The switching operation of the converter leads to high currents between the capacitive and inductive components on the PCB, these currents induce electromagnetic fields which have to be reduced to minimize effects on other circuits and the operation of the circuit itself.

2. The trace from the DC-DC converter IC to the switching transistor contains high frequencies due to the fast switching operation and must be kept as short as possible.

3. The feedback voltage network is sensitive to noise and must be placed as close as possible to the feedback pin of the DC-DC converter IC. It must be treated as analog circuit and protected from high noise interference.

Figure 4.2 shows the final layout of the step-down DC-DC converter switch-mode power supply. The green lines indicate the main current loops. On the output side of the transformer these are the loops through the inductor (transformer), the diode and the main output capacitor. On the input side the loop starts at the input capacitor, goes through the controller IC and the primary winding of the transformer, to the output capacitor and on the ground plane back to the input capacitor.

The switch node (red rectangle) is kept as short as possible to minimize noise transmission by the high switching frequencies. The feedback network (blue polygon) is placed as close as possible to the respective pins of the controller IC. This reduces effects caused by induced noise on the feedback voltage.

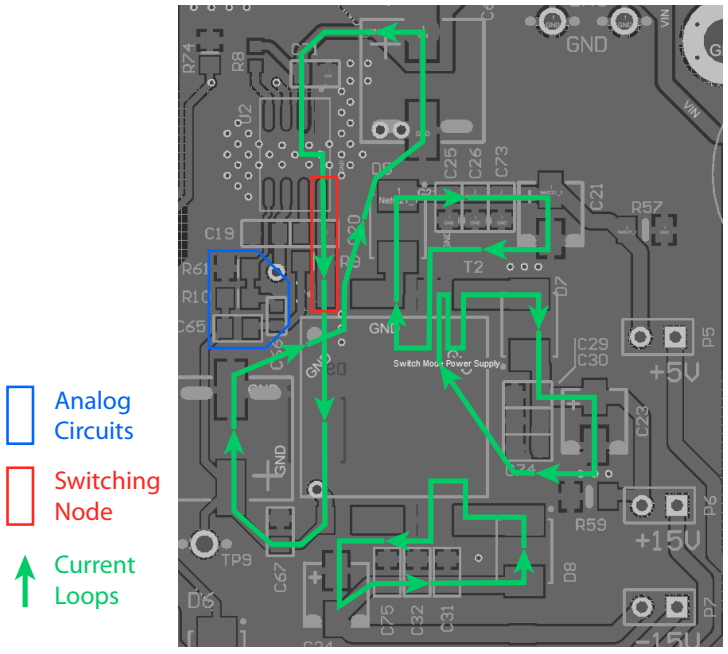

Figure 4.2.: Layout of the step-down DC-DC converter.

The controller IC LM5017 has a solder pad on its bottom to improve heat extraction from the IC. Further improvements to heat extraction are made by connecting the ground planes on the top and bottom copper layers in the area around the controller IC using thermal stitching vias with a hole size of 0.35 mm. This leads to an increased total copper area, absorbing the heat and therefore a better thermal capacity.

Beside the output capacitor components included in the schematic of the switch-mode power supply, solder pads for two additional capacitors in a standard 0805 package are included in the layout for each output branch to allow placement of ceramic capacitors to shortcut high frequencies produced by the switching operation of the circuit. The value of these capacitors is dependent on parasitic effects of the components, their placement and the layout itself and can not be determined though simulations in advance, but must be measured using an assembled prototype.

4.2.2 Layout of the High-Voltage Step-Up Switch-Mode Power Supply

For the design of the high-voltage step-up converter switch-mode power supply layout, the same considerations have to be taken into account as for the switch-mode power supply for the lower voltages. The components used in this circuit block are considerably larger than these used in the low-voltage power supply block. Therefore the current paths as shown in figure 4.3 are naturally larger as well. The output current loops use the bottom plane of the PCB for ground return currents (dashed lines in figure 4.3). The placement of the components is greatly influenced by their size and the position of the respective connectors. The resulting placement is not beneficial for the goal of keeping high power currents away from sensitive analog circuit parts (blue polygon), but a compromise of all the relevant factors. To still protect the analog circuit blocks, the ground planes on the top and bottom layer are dissected around the controller IC including all sensitive circuit parts. The separated ground planes are connected to the surrounding ground plane close to the input capacitor C_2.

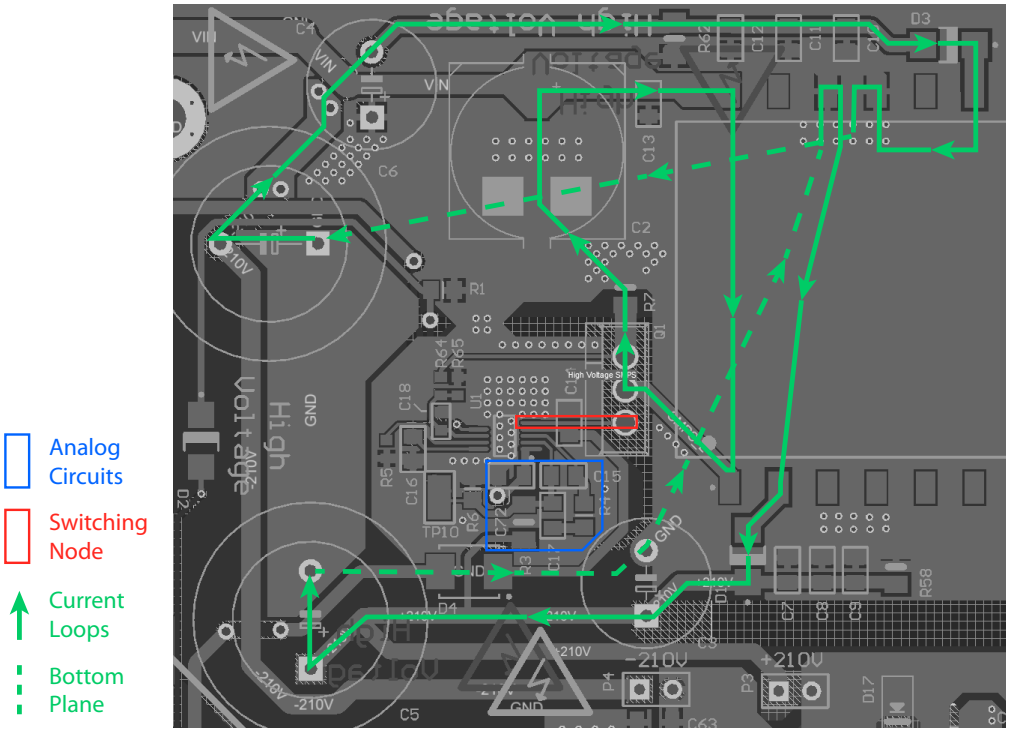

Figure 4.3.: Layout of the high-voltage step-up DC-DC converter.

The placement of the components takes thermal considerations into account freeing the area next to the switching transistor for the possibility to attach a heat sink to the transistor. Heat abstraction from the controller IC is fostered by thermal vias underneath and around the IC to increase the thermal capacity of surrounding (ground) copper planes.

For each output voltage solder pads for three additional capacitors in standard `0805` package are added to the layout to provide means for shortcutting high frequency noise on the output traces determined by measurements on an assembled prototype.

4.2.3 Layout of the Operational Amplifier Block

The operational amplifier is split into two sections depending on the maximum voltage involved in the respective circuit block. Figure 4.4 shows the layout of the complete operational amplifier block. The left side contains the low-voltage components with maximum voltages up to ±15 V. The right side contains the high-voltage output amplifier block. The output of the integrated operational amplifier drives the high-voltage block through resistor R_{46}. The feedback is returned to the integrated operational amplifier through the lower resistor of the voltage divider (R_{53}) and capacitors C_{53} and C_{60}.

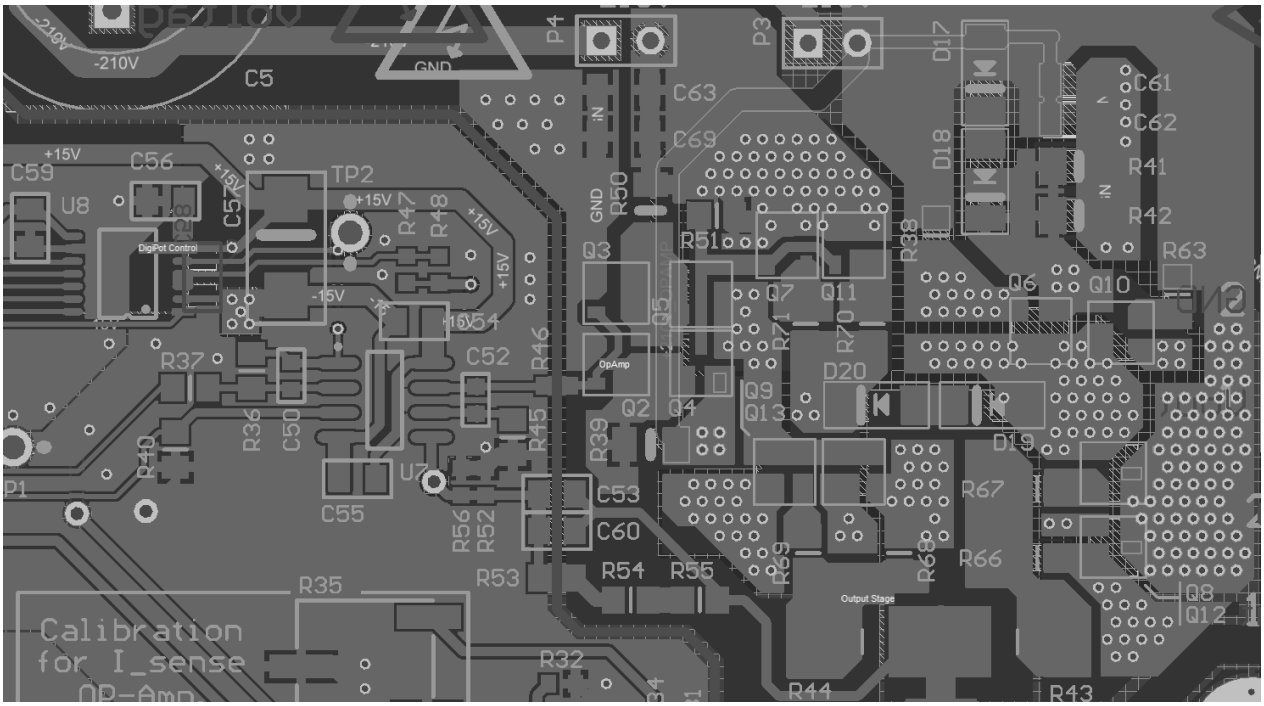

Figure 4.4.: Layout of the operational amplifier.

The digital potentiometer (U_8) is placed at the top left in figure 4.4, because it has a digital control interface and is part of the analog connection between the two integrated operational amplifier stages. This way the digital interface (on the left) stays at maximum distance to the analog signals.

The output of the high-voltage amplifier block is at the bottom right in figure 4.4 at center tap between the two high power 2 W, 100 Ω resistors (R_{43} and R_{44}). The layout of the output stage is designed to minimize trace lengths. The traces itself are made as wide as possible to increase the thermal capacity of copper areas connected to the transistors. The structural shape of the transistors does not allow attachment of heat sinks, therefore the device terminals are the only way to extract heat from the components. Copper

planes around the transistors are made as large as possible and connected to the copper areas on the bottom layer to increase their thermal capacity.

4.2.4 Layout of the Current Sense Amplifier Block

The layout of the current sense amplifier is shown in figure 4.5. The critical part is the voltage divider connected to the input terminals of the amplifier (highlighted in red). The traces from shunt resistor R_{29} on the right to the amplifier inputs are kept as short and symmetric as possible. The signal on these traces is sensed as differential signal. Therefore, if noise or external influences are induced at all, they should be induced on both traces in the same way. The upper resistors of the voltage divider (R_{30} and R_{31}) bridge the high-voltage section on the right and the low-voltage section containing the current sense amplifier on the left.

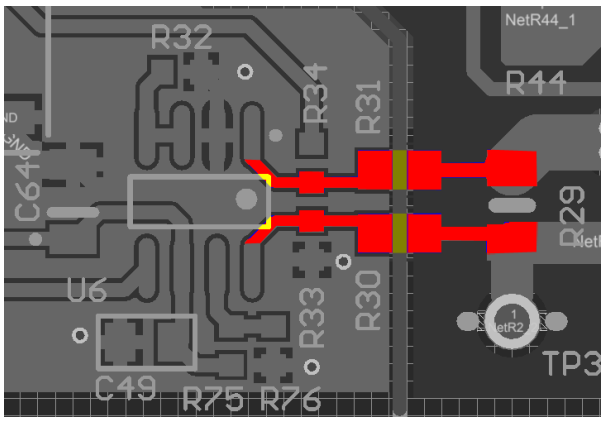

Figure 4.5.: Layout of the current sense amplifier.

4.2.5 Layout of the Digital Control Circuits

4.3 Controller Board

The layout of the controller board is less complex than the layout of the driver board. The controller board contains the input power connectors with reverse voltage polarization protection on the left ("Input"), the switch-mode power supply circuit for the 3.3 V supply voltage generation ("SMPS") on the top left, the digital control circuit ("Digital") in the center of the board and the USB connection on the right. The four channels for the connection of driver boards are placed on the top and bottom of the board with the respective transceiver ICs next to the connectors.

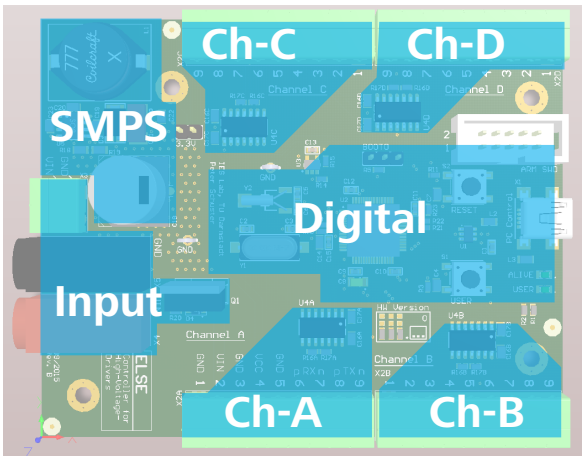

Figure 4.6.: Placement of circuit building blocks on the controller board.

Mapping of the UART peripheral instances of the microcontroller to the connection channels is made to minimize traces lengths on the PCB and simplify the layout. Channel A is connected to UART 2, channel B is connected to UART 3, channel C is connected to UART 4 and channel D is connected to UART 1.

The design considerations regarding the layout of the 3.3 V switch-mode power supply block are in general the same as for the two previously discussed switch-mode power supply layouts. The major difference is that this power supply block follows the design of a standard step-down DC-DC converter with a single inductive element, compared to the previously discussed designs featuring transformers. Therefore two main current paths exist and need to be taken into account. The current loop being active when the transistor is switched on is marked in green in figure 4.7. It origins in the input capacitor, goes through the controller IC, through the inductor to the main output capacitor, and the return current on the ground plane goes back to the input capacitor. The other current loop is active during the off state of the transistor. It is marked in orange in figure 4.7 and includes the diode, the inductor and the output capacitor. Design goal for the layout is to have as much overlap as possible between these two current paths and minimize the area wrapped by the current loops.

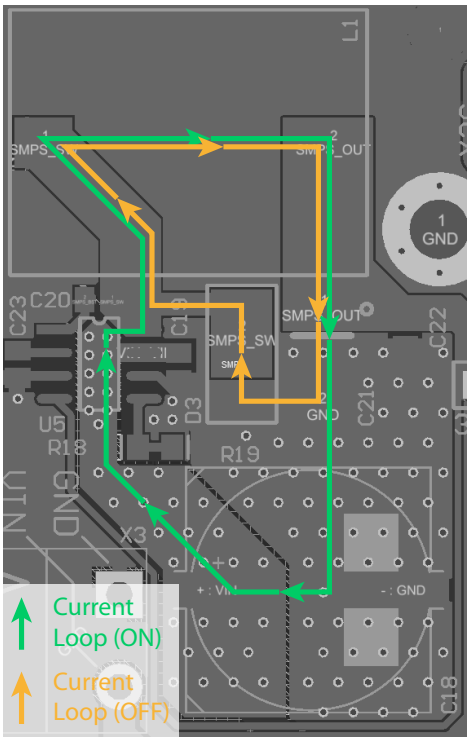

Figure 4.7.: Layout of the 3.3 V switch-mode power supply.

The used controller IC `MAX5035` does not require analog support circuitry. Therefore, protection of analog circuits does not need to be taken into account.

5 Software

The designed hardware systems on the controller and on the driver board, contain a microcontroller as central component of the control circuitry. Operation of this general purpose microcontroller is defined by the software it executes. The following chapter discusses the design and properties of the software developed for both systems and the protocols in place to allow communication between these systems and between the controller board and a connected computer for general control.

5.1 Communication Protocols

The software systems on the driver and control boards communicate with each other using a custom control protocol. The design of this protocol is discussed in section 5.1.2. For the communication of the controller board with a connected computer a second protocol is implemented and discussed in section 5.1.1.

5.1.1 Controller-PC Communication

Major design goal for the communication protocol between a computer and a controller board is easy readability by humans and the possibility to enter all relevant commands by hand on a terminal window providing simple access to the serial connection between the computer and a controller board. To meet this design goal all commands contain only *ASCII* characters. The carriage return (`\r`) character is used as termination character indicating the end of a command or message.

The protocol follows a strict request-response design. The computer issues requests to the controller system and retrieves responses accordingly. The controller system does not send messages without being requested to do so by the computer and does not send requests to the computer by itself.

The commands defined in the protocol are categorized in two, orthogonal groups. Every command is either a *get* command to retrieve information from the system or a *set* command to change parameters of the system. Commands can furthermore target either the controller board or one of the connected driver boards. All commands start with an operation code build from these two groups and an additional character identifying the operation in the respective group. The first character determines whether the operation is a *get* (`G`) or a *set* (`S`) operation. The next three characters specify the target of the command: controller (`CTR`) or driver (`DRV`). This leads to the following canonical format: `[G|S][CTR|DRV]x` with `x` being an additional character identifying the action that is to be performed on the target device.

Return messages do not follow a strict format in general, but are human readable messages. Two standard return messages exist, when no further information is returned by the system: `OK` and `ERR`. When the transmitted command is not known or not in a valid format, a special `INV OP` message is returned by the controller.

Messages in both directions can contain parameters following the command code. Parameters are delimited by spaces (character 20: `' '`).

The following sections document all defined control messages with possible parameters and allowed return messages.

Get Controller Info (GCTRI)

The *Get Controller Info* (GCTRI) command is a *get* command to retrieve general information (I) from the controller (CTR). No further parameters are allowed for this command.

The result returns hardware and firmware version of the controller and follows the format `FW [Version] HW [Version]`. The hardware version starts at 0, the firmware version starts at 1. An example response is `FW 001 HW 001`.

Get Drivers (GCTRD)

The *Get Drivers* (GCTRD) command is a *get* command to retrieve a list of all connected driver boards from the controller. No further parameters are allowed for this command.

The result is a list of all driver boards connected to the controller and follows the format `[CH]-[ID] [CH]-[ID] [CH]-[ID]`. `CH` indicates the respective channel number (`A` to `D`) and `[ID]` indicates the assigned id inside of this channel. Ids start at 1. An example response is `A-01 A-02 C-01 D-01`.

Get Driver Info (GDRVI)

The *Get Driver Info* (GDRVI) command returns the `CPU ID` of the driver specified by the channel number and id included as parameter to the command. The general format of the command is `GDRVI [CH]-[ID]`. An example request message is `GDRVI C-03`.

The response to the command contains the `CPU ID` of the respective driver in hexadecimal format. The general format of the response is `CPU-ID [cpu id hex]`. An example response is `CPU-ID 0xA1B2C2D3`.

Get Driver Status (GDRVS)

The *Get Driver Status* (GDRVS) command returns information about the current status of the driver specified by the channel number and id included as parameter to the command. The general format of the command is `GDRVS [CH]-[ID]`. An example request message is `GDRVS B-01`.

The response to the command contains a number of internal parameters of the driver. The information includes the power status of the switch-mode power supplies on the board represented as 0 or 1, the status of the arbitrary waveform generator represented as 0 (idle) or 1 (running), the configured waveform with the following allowed values: sine (0), square (1) and triangular (2). The next parameter is the frequency in decimal form, followed by the scale factor set to the digital potentiometer with allowed values from 0 to 1023. The last parameter contains a scale factor applied to the original waveform template in fractional form. The format for this parameter is `[Numerator]/[Denominator]`. The response contains these described parameters and follows the form `[PWR] [AWG] [Wave] [Freq] [Scale] [Factor: Num/Den]`. An example response is `1 0 1 1000 650 1/1`.

Set Driver Config (SDRVC)

The *Set Driver Config* (SDRVC) command sets all parameters of a driver board required to generate arbitrary waveforms. First parameter to the command is the channel and id of the addressed driver board. The next four parameters define the selected waveform, the frequency, the gain factor, and scale factor for the

waveform template. The format of these parameters is identical to the parameters in the response to the *Get Driver Status* (GDRVS) command shown previously. All parameters must be specified. The format of the command is SDRVC [CH]-[ID] [Wave] [Freq] [Scale] [Factor: Num/Den]. An example command is SDRVC A-01 1 1000 650 1/1.

The controller responds with OK or ERR depending on the success of command execution.

Set Driver Power (SDRVP)

The *Set Driver Power* SDRVP command enables or disables the power supply circuits on the driver board specified as first parameter to the command. The general format of the command is SDRVP [CH]-[ID] [1|0]. An example command is SDRVP A-01 1.

The controller responds with OK or ERR depending on the success of command execution.

Set Driver AWG (SDRVA)

The *Set Driver AWG* (SDRVA) command enables or disables the arbitrary waveform generator on the driver board specified as first parameter to the command. The general format of the command is SDRVA [CH]-[ID] [1|0]. An example command is SDRVA A-01 1.

The controller responds with OK or ERR depending on the success of command execution.

5.1.2 Board-to-Board Communication

The protocol used for communication between the driver and controller boards involves no manually crafted messages or human interactions. Implementation of the protocol and handling of message at the endpoints should require as less RAM as possible, due to the limited amount available on the driver boards. It also needs a mechanism to detect collisions, possibly caused by multiple endpoints on the bus sending at the same time. The protocol also needs to provide means for addressing of driver boards to send messages directed at a specific driver board and to identify the sending driver board on the controller side. To satisfy the requirement for small RAM usage, the protocol is not *ASCII* based, but message handling and processing is done on bit/byte level. In the following section all message data is therefore displayed in hexadecimal encoding. The second requirement for collision detection is implemented by Cyclic Redundancy Check (CRC) checksums included in the messages.

All messages following the communication protocol for board-to-board data exchange follow the same general structure: the fist byte contains the command code as an unique identifier for the message type, the last byte contains the hexadecimal value 0xFF to indicate the end of the message. The byte right before the last byte contains the CRC checksum over all data up to the byte containing the checksum to enable collision detection at the sender. Data spanning multiple bytes is encoded following the little-endian representation. The UART is operated with 8 data bits, no parity bits and one stop bit. The baud rate for the UART is 38,400 baud/second.

Driver boards need to announce their presence to the controller board to be addressable by the control computer. Therefore, a registration mechanism is implemented as part of the protocol. The driver sends a registration message (REG command) containing its globally unique 32-bit CPU id to the controller. The controller assigns an id to the driver (ID command) which is used thereon as unique id by the driver to

identify itself to the controller and to identify messages directed at itself. The CPU id is included in the `ID` message as well to enable driver boards to identify the intended receiver of the message.

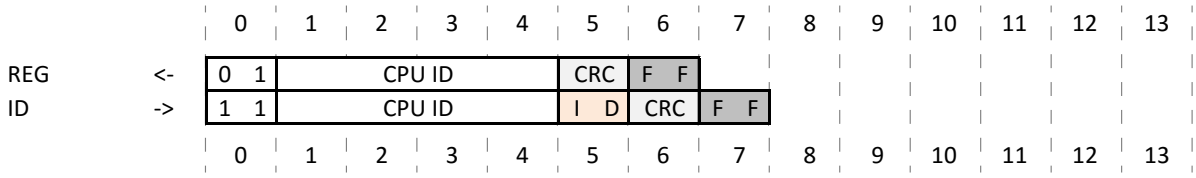

Figure 5.1.: Board-to-Board communication: registration messages.

All further control, request and information messages contain the unique id of the sender for messages sent by the driver or the id of the receiving driver when the message is sent by the controller as second byte following the command code.

A driver responds to control messages sent from the controller with three possible messages. When the sent command can not be executed by the driver an "Invalid Operation" (`INV OP`) message is send in return. When the command is executed successfully an "Acknowledged" (`ACK`) message is send in return. When a driver receives an invalid formatted or unknown message it sends a "Not-Acknowledged" (`NACK`) message in return.

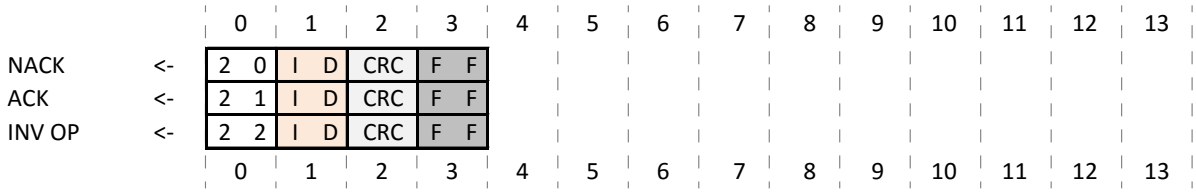

Figure 5.2.: Board-to-Board communication: response messages.

The four general control messages `PWR OFF`, `PWR ON`, `AWG OFF`, and `AWG ON` control the behavior of a driver board. `PWR OFF` deactivates the power supply blocks on the driver board. `PWR ON` activates the power supply blocks on the driver board. `AWG OFF` deactivates the arbitrary waveform generator on the driver board. `AWG ON` activates the arbitrary waveform generator on the driver board. Messages listed in figure 5.2 are send in return.

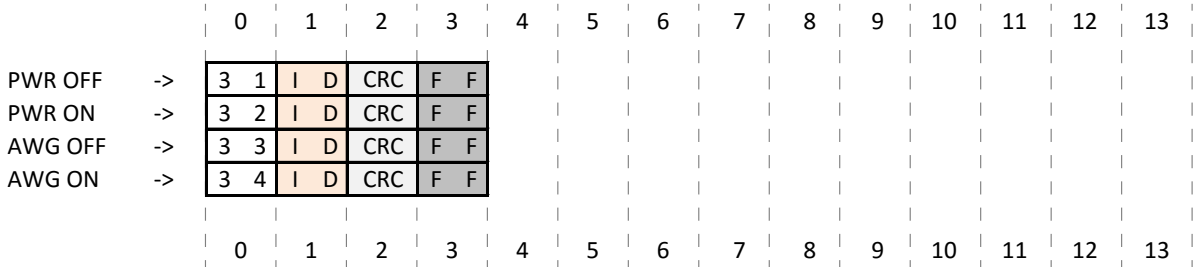

Figure 5.3.: Board-to-Board communication: control messages.

A set of configuration messages can be used to configure the parameters of the arbitrary waveform generator on a driver board. The `WAVE` command is used to configure the selected waveform. Allowed values are sine (0), square (1) and triangular (2). The `FREQ` command is used to set the output frequency

of the arbitrary waveform generator. The frequency is represented as a 16-bit value. The `SCALE` command is used to set the gain factor. Values in the range from 0 to 1023 are allowed. The value must be encoded as a 16-bit value. The `FACTOR` command is used to set the scale factor applied to the waveform template selected by the `WAVE` command. The scale factor is represented as a fractional number build from an 8-bit numerator and an 8-bit denominator.

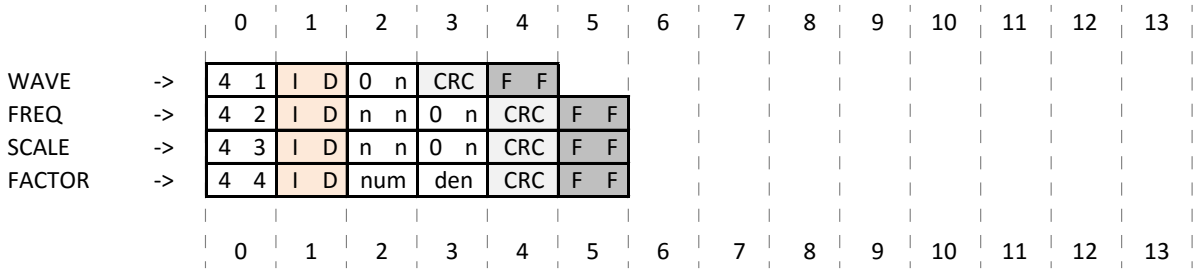

Figure 5.4.: Board-to-Board communication: configuration messages.

An `INFOQ` command is sent to a driver board to request a report of the internal status of the system. The response is an `INFO` message containing an 8-bit firmware version, an 8-bit hardware version, the status of the power supply blocks (1 or 0) encoded as 4-bit number and the status of the arbitrary waveform generator (0 for *idle* and 1 for *running*). Furthermore the internal parameters of the arbitrary waveform generator are included in the `INFO` message. Their representation and encoding is the same as for the configuration messages (figure 5.4).

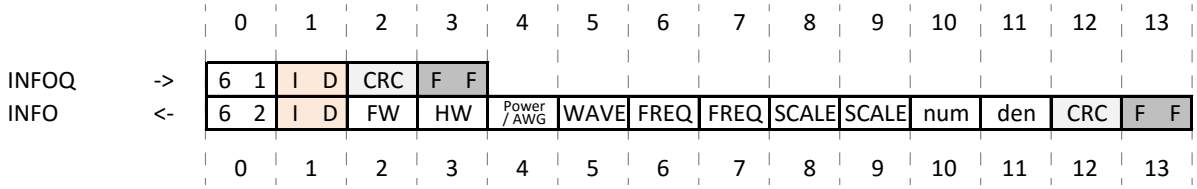

Figure 5.5.: Board-to-Board communication: information request messages.

When a receiver detects a collision it informs the sender with a `NACK` message. The nature of collisions is that more than one sender is active on the bus, but the receiver can decode only one sender id of the message. Therefore, senders need to implement a mechanism to detect timeouts for expected responses and retransmit their original request messages. Collisions can occur only on the transmission line used by the driver boards (see section 3.6.4). Therefore only the controller needs to implement mechanisms to detect collisions.

Disconnected driver boards are not detected by the controller immediately. A possible extension of the protocol would therefore be a *ping* mechanism to regularly query drivers for their presence and discard their registrations at the controller side, if no response to a *ping* message is received.

5.2 Driver Board Firmware

Source code of the firmware for the driver board is contained in the digital media submitted as part of this thesis and can thereby be viewed in full extent. The following sections discuss the architecture of the system, the general functionality of the included components and characteristics of the system resulting from distinct design decisions and implementation details.

The system is divided into four major functional blocks: a component dealing with receiving, sending and processing messages (`COMM`), a block controlling the DAC (`AWG`), a block interfacing with general hardware components of the microcontroller (`HW`) and a block configuring the connected digital potentiometer (`DigiPot`).

The following diagram illustrates the general architecture of the system. Peripheral components being part of the microcontroller are included with white fill, software modules abstracting the functionality of these hardware modules are represented with light-grey fill. Software modules to be possibility added in future revisions of the firmware are included in the diagram and indicated by a grey border.

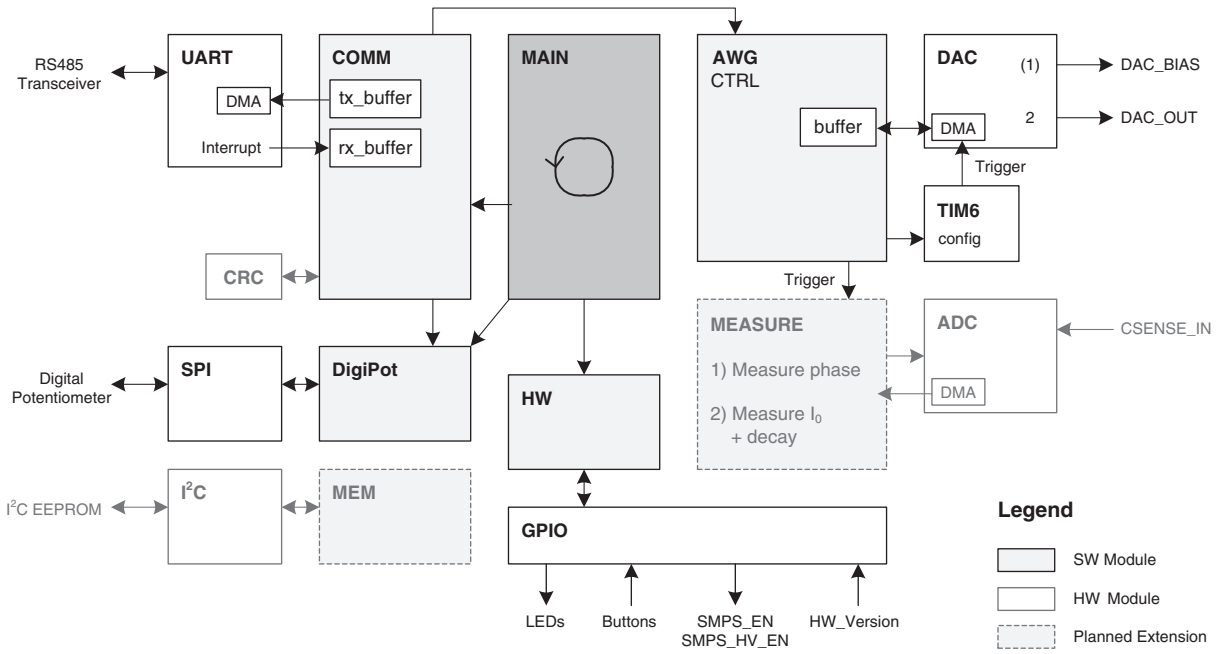

Figure 5.6.: System architecture of the driver board firmware.

The software *STM32CubeMX* by *STMicroelectronics* is used to configure the used hardware peripherals and the clock tree and generate a template containing a general hardware abstraction layer and template files for the software of the driver board.

Figure 5.7 shows the clock configuration of the microcontroller based system on the driver board as done in the *STM32CubeMX* software. The 8 MHz external oscillator clock is selected as input into a PLL and multiplied by 6 to generate the 48 MHz system clock. The 32.768 kHz external low frequency oscillator is selected for the real-time system of the System-On-Chip.

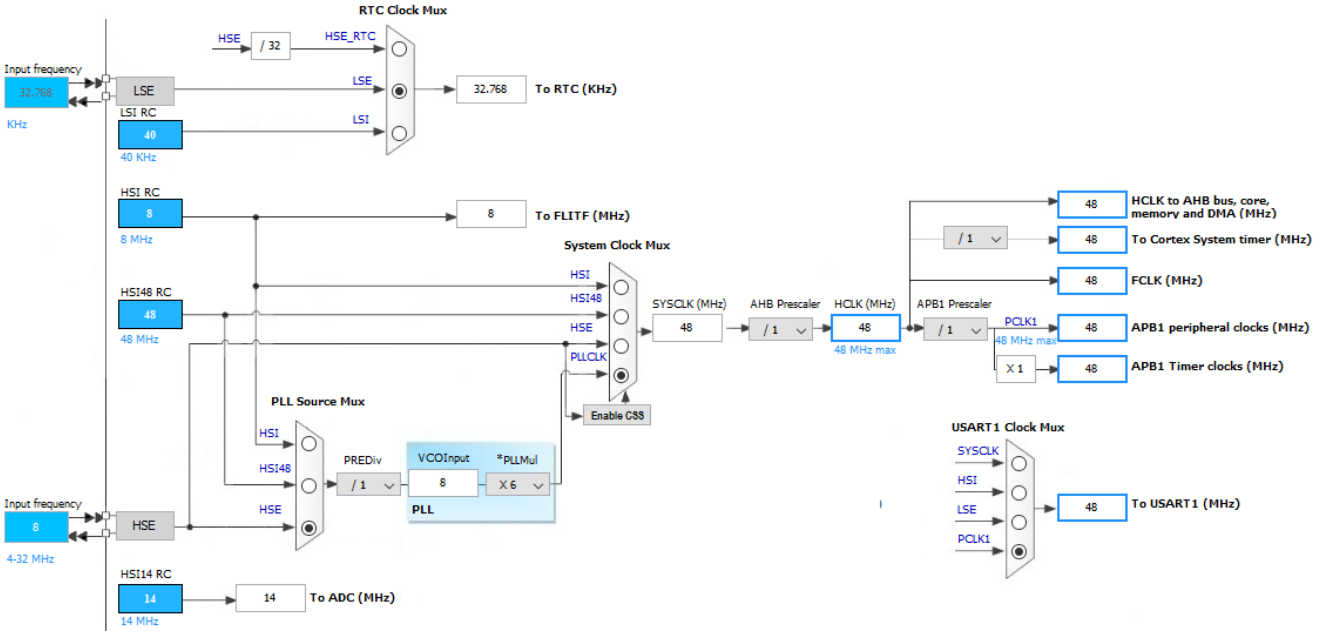

Figure 5.7.: Clock configuration of the driver board firmware.

Once initialized, the system is controlled by the communication module through incoming messages or pressing the *user* button on the board. The *main loop* runs in an infinite loop and triggers processing of received messages and reads the status of the pin connected to the *user* button continuously. The following sections describe the functionality included in the four main firmware modules previously introduced.

5.2.1 Arbitrary Waveform Generator

The arbitrary waveform generator (`AWG`) block controls the operation of the DAC hardware peripheral on the microcontroller.

A set of methods enables other components in the system to set configuration parameters or retrieve current values of distinct parameters. This includes the selected waveform, the scale factor as fractional number to be applied to the template of the selected waveform and the output frequency.

```
void AWG_SetWaveform(AWG_Waveform waveform);
AWG_Waveform AWG_GetWaveform();

void AWG_SetScaleFactor(uint8_t numerator, uint8_t denominator);
AWG_ScaleFactor AWG_GetScaleFactor();

void AWG_SetFrequency(uint16_t frequency);
uint16_t AWG_GetFrequency();
```

The three methods `AWG_Start`, `AWG_Stop`, and `AWG_GetStatus` are used to start and stop the waveform generator and to retrieve the current status (idle or running).

```
void AWG_Start();
```

```
void AWG_Stop();

AWG_Status AWG_GetStatus();
```

The DAC can operate with a resolution of 12-bit and a maximum sample frequency of 1 MHz. The waveform generator firmware uses embedded waveform data as template for the generated output. Figure 5.8 shows the three embedded waveforms: sine, rectangle and triangle. The templates are embedded with 400 samples per period and full 12-bit resolution.

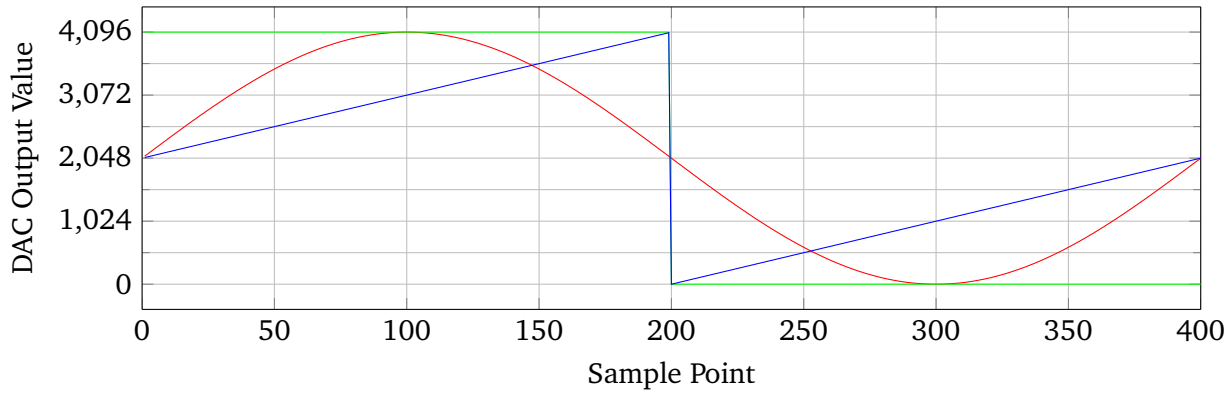

Figure 5.8.: Waveform templates embedded into the driver board firmware.

The predefined number of 400 samples per period allows a maximum output frequency of 2,500 kHz resulting in a sample frequency of 1 MHz. When the selected output frequency multiplied with the samples per period exceeds 1 MHz, the number of samples per period is divided by two until the resulting sample frequency is less or equal to 1 MHz. This allows the system to take predefined data from the templates also for higher output frequencies without the need for interpolating points in-between the defined data points in the template.

An example illustrates this mechanism: For a selected output frequency of 3,000 kHz the sample count per period is reduced to 200. This yields a sample frequency of 600 kHz which is below the maximum sample frequency of 1 MHz. With the computed number of 200 samples per period every second data point in the waveform template is skipped. This results in the desired waveform, but the signal is generated with reduced horizontal resolution due to the limited sample frequency of the DAC.

Selection of the output voltage is primarily done by setting the gain factor of the operational amplifier block. This is accomplished by changing the value of the digital potentiometer, but due to the limited gain factor range, only the upper output voltage range can be covered with a full 0 to 3.3 V signal at the input of the operational amplifier block. To generate an output signal with low peak-to-peak output voltage, the input signal to the operational amplifier block must be generated with a lower amplitude. Therefore the *scale factor* parameter of the arbitrary waveform generator allows scaling the waveform template before sending it to the DAC hardware block. The *scale factor* is a fractional number with 8-bit numerator and 8-bit denominator by which the sample points in the template are scaled. The waveforms embedded as templates are centered at 2048 which represents the ground potential of the output signal. Applying a scale factor to one of the templates by multiplying each data point with the provided factor leads to a shifted mean value of the waveform. This effect is compensated by adding an additional offset to the scaled data points shifting the new waveform back to a correct mean value of 2048. The offset o is calculated from the scale factor f using the following equation

$$o = 2048 \cdot \left(1 - f\right). \tag{5.1}$$

After the data points for the set parameters are calculated and written to an internal buffer, the DAC is configured to read its data from the internal buffer using Direct Memory Access (DMA). The buffer is treated as circular buffer, yielding a continuous period signal at the output of the DAC. Timer 6 of the microcontroller is configured to the calculated sample frequency and triggers the DAC to increase the memory address inside the buffer to output the next sample point. A second DAC channel is set to a value of $4095/3 = 1365$ to provide a fixed offset for the signal balancing stage of the operational amplifier (see section 3.1.1).

The trigger signal of timer 6 is generated by a counter inside the timer counting up on every clock tick until a preset value is reached. When the preset value is reached, the trigger signal is sent to the DAC and the same process starts again. The preset value (P) can be calculated from the clock frequency (C), the sample frequency (S), defined by sample count N and output frequency F as

$$P = \frac{C}{S} = \frac{C}{N \cdot F} = \frac{48{,}000}{N \cdot F}. \tag{5.2}$$

All parameters of this $1/x$ function are natural numbers, therefore not all output frequencies can be generated by the timer. For low output frequencies (large timer preset values) a high precision can be achieved, but for lower timer preset values not all frequencies can be generated. One approach to optimize this behavior is to change the number of samples per period to arbitrary values, but this would require interpolation of data points of the waveform and is therefore not implemented in this system.

5.2.2 Control of the Digital Potentiometer

The digital potentiometer (`AD5293`) is controlled using the integrated SPI peripheral block. The SPI peripheral is configured for an interface clock speed of 12 MHz and 16-bit data words with endianess set to *Big Endian* (most significant byte first). The firmware block encapsulating this functionality contains three functions for access by other software components of the system. The `DigiPot_Enable` function performs an initialization of the digital potentiometer by sending a number of commands defined in the datasheet to the digital potentiometer IC [6, table 11, p. 19].

Command `0x1802` enables an update of the resistor value. The value of the resistor is set by sending the result of an inclusive disjunction of the command `0x0400` with the value of the resistor register in the range between 0 and 1023. This functionality is encapsulated inside the function `DigiPot_SetValue`. The function `DigiPot_GetValue` returns the current, cached value of the resistor register.

5.2.3 Hardware Module

The hardware module (`HW`) encapsulates access to microcontroller pins. This includes enabling and disabling LEDs and the power supply blocks on the driver board and reading the status of the *user* button and hardware version number set by the respective external resistor network. The hardware module also resets the `TX` and `RX` LEDs, indicating transmission and arrival of messages over the RS485 interface, one second after they were set by the communication module and measures the time in milliseconds the *user* button was pressed. Timed actions are evaluated and eventually triggered by the `HW_Tick`

function which tracks and calculates elapsed time spans by using the system tick counter. The system tick counter is operated by the system tick interrupt handler which is called every millisecond by the CPU. The `ALIVE/BLINK` LED is also operated by this function.

5.2.4 Communication Module

The communication module (`COMM`) receives data from the controller board using interrupts. The data is received byte by byte and added to a ring buffer. When a packet end (byte `0xFF`) is recognized the receipt of a full packet is signaled to the system and processed from thereon. Processing of the received packets in done outside of the interrupt service routine receiving the bytes from the UART interface and adding them to the ring buffer and has to be triggered from the *main loop*.

Processing received packets starts with copying the message data to a separated buffer to free space in the ring buffer used for receiving data and simplify message processing by enabling data access to continuous memory space. Received packets are filtered by driver board id or CPU id as specified in the protocol description and only processed, if they are directed at the current driver board.

Depending on the command contained in the received message, the communication module sets parameters of the arbitrary waveform generator (`AWG`) the digital potentiometer (`DigiPot`) or enables or disables the power supply blocks on the board. Received and filtered messages are signaled to the controller board by sending `ACK`, `NACK`, and `INV OP` according to the protocol specification (section 5.1.2).

On start-up the system does not have a driver board id, yet. Therefore, it sends a `REG` message to the controller board announcing its presence until it receives an id from the controller board.

5.2.5 Evaluation

The implemented firmware has a size of 19616 byte and requires 7360 byte of RAM to run. The microcontroller on the driver board has 128 KB of flash memory and 16 KB RAM. This leaves a lot of room for extensions of the firmware, adding further functionality. A few ideas are already shown in figure 5.6 but possibilities for extension are not limited to these. Additionally it is possible to exchange the microcontroller with a model being part of the same series, but equipped with less flash memory, as drop-in replacement to save component costs.

5.3 Controller Board Firmware

Sole purpose of the microcontroller on the controller board is to act as a communication hub between the computer connected via USB and the driver boards. The firmware developed to achieve this is split into two main modules. Figure 5.9 shows the architecture of the firmware deployed on the microcontroller on the controller board. A *USB communication module* (`USBU`) is responsible for receiving and transmitting data over the USB interface. The *UART communication module* (`DRV`) on the other side is responsible for sending and receiving data over the four UART interfaces. It also manages the connections to the connected driver boards. Access to low-level hardware functions is implemented in the `HW` module identical to the firmware on the driver board.

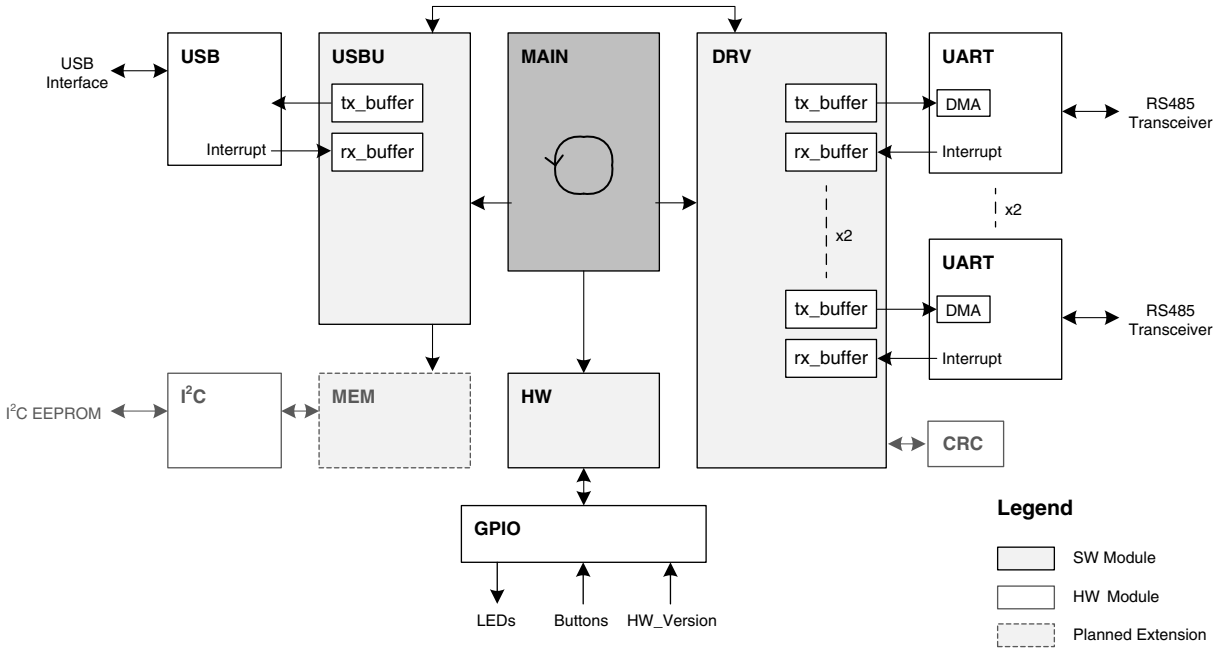

Figure 5.9.: System architecture of the controller board firmware.

Figure 5.10 shows the clock configuration of the microcontroller based system on the controller board as done in the *STM32CubeMX* software. The 8 MHz external oscillator clock is selected as input into a PLL and multiplied by 9 to generate the 72 MHz system clock. A pre-scaler with factor 1.5 yields the required 48 MHz clock for the USB sub-system. The 32.768 kHz external low frequency oscillator is selected for the real-time system of the System-On-Chip.

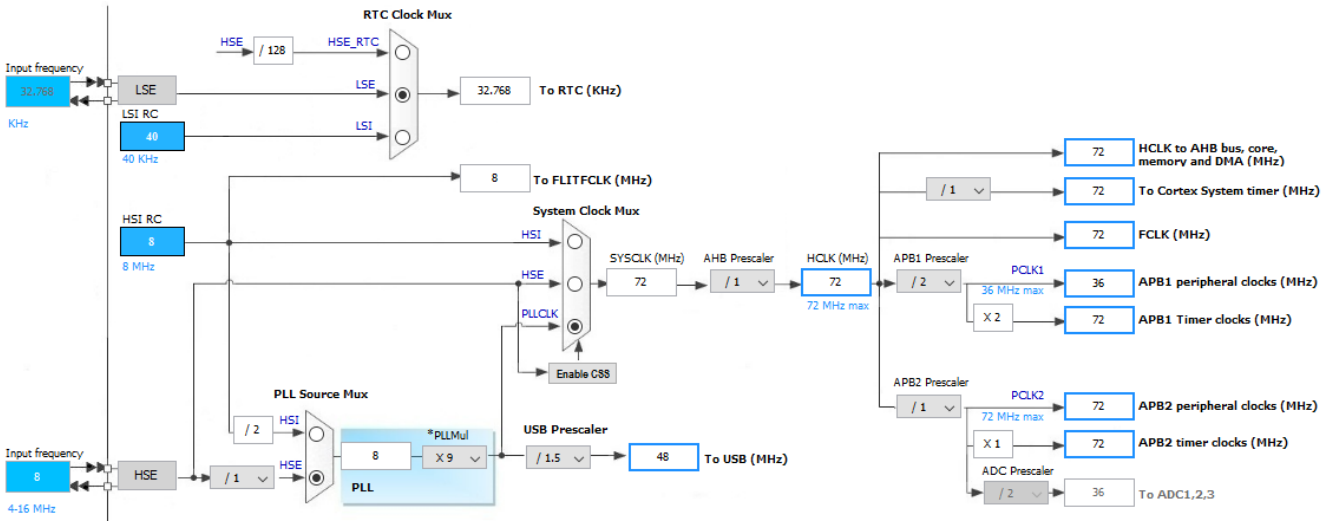

Figure 5.10.: Clock configuration of the controller board firmware.

Once initialized the system is controlled by the two communication modules through incoming messages. The *user* button on the board is not used as trigger for any functionality, yet. The *main loop* runs in an infinite loop and and triggers processing of received messages continuously.

5.3.1 USB Communication Module

The USB peripheral is configured as *communication device class* (CDC) device. Therefore, the USB drivers provided by *STMicroelectronics* expose the USB interface as emulated serial connection to the operating system on a computer and commands to the controller board can be sent using any terminal control software or any other software enabling the user to send messages over serial connections. Responses from the controller board are received the same way.

Main purpose of the USB communication module in the controller board firmware is to extract the numeric values from received *ASCII* messages and forward the raw data to the UART communication module. When the UART module forwards messages to the USB communication module the raw data is encoded to *ASCII* messages and sent to the connected computer.

5.3.2 UART Communication Module

The UART communication module manages connections to all connected driver boards over four communication channels using four distinct UART peripheral blocks. The state of every communication channel is stored in a separate instance of a *struct* with the following definition:

```
typedef struct {
    UART_HandleTypeDef* huart;
    uint32_t clients[DRV_PER_CHANNEL];
    uint8_t tx_buffer[DRV_TX_BUFFER_LENGTH];
    uint8_t rx_buffer[DRV_RX_BUFFER_LENGTH];
    uint16_t tx_length;
    uint16_t rx_pointer;
    uint16_t rx_length;
    uint8_t rx_byte;
    DRV_TxStatus tx_status;
    uint32_t tx_send_time;
    uint8_t tx_send_count;
    DRV_RxStatus rx_status;
    DRV_RxProcessingStatus rx_proc_status;
    uint8_t rx_overflow[DRV_RX_OVERFLOW_LENGTH];
    uint8_t rx_overflow_p;
    drv_tx_config_t config_buffer;
} DRV_Channel;
```

The `huart` variable stores a pointer to the respective UART peripheral used for sending and receiving data on the channel. The `clients[]` array stores the CPU id of all registered clients on this channel. The index of an entry in the array added with a fixed offset of one represents the session id of this client. All received bytes are stored in a buffer and processed as soon as a message end byte (`0xFF`) is recognized. When the system receives further data while the current message is still processed, these bytes are stored in an overflow buffer (`rx_overflow[]`).

Messages to be send through a UART communication channel are stored in the transmission buffer (`tx_buffer[]`). A message is kept in this buffer and resent every 500 ms until an `ACK` message is received from the respective driver board. The `tx_send_time` variable contains the timestamp of the last

transmission in system ticks. When a message is sent 10 times without receiving an `ACK` message from the targeted receiver, the message in the buffer is discarded and the `tx_status` variable reset. The `tx_status` variable is also reset when an `ACK` message is received. When an `INV OP` message is received in response to a transmitted message an `ERR` message is send to the computer through the USB communication module.

The communication protocol used on the USB interface sends and receives configuration data of the driver boards in a single message. The communication protocol used on the UART interface uses one message for every configuration parameter, on the other hand. Therefore, the `config_buffer` variable in the above *struct* is used to store partially received or transmitted configuration data until all required messages are send or received over the UART interface.

5.3.3 Evaluation

The implemented firmware for the controller board has a size of 25604 byte and requires 9556 byte of RAM to run. The microcontroller on the driver board has 1 MB of flash memory and 96 KB RAM. This leaves a lot of room for extensions of the firmware, adding further functionality. It is also possible to exchange the microcontroller with a model being part of the same series, but equipped with less flash memory, as drop-in replacement to save component costs.

6 Evaluation

During the course of the project a first prototype of the driver board was build, thoroughly tested, and all findings were incorporated in a second version of design and layout of the driver board. The measurements done on the second prototype build after incorporating these findings are discussed in the following chapter.

One prototype of the controller board was assembled and tested. Measurements done on this prototype are included in the following chapter as well.

6.1 Switch-Mode Power Supplies

Functionality of the switch-mode power supplies involves high voltages, currents, and frequencies and is therefore one of the most critical aspects of the built system. The following figures show measurements performed with an oscilloscope in the time domain. For all measurements the minimum required input voltage of 24 V is used.

Figure 6.1 shows measurements performed on the *LX* (switching) output of the 3.3 V DC-DC step-down controller IC (channel 1) and at the generated 3.3 V output voltage (channel 2). Following the volt-time principle, the duty cycle for an input voltage of 24 V and an output voltage of 3.3 V should be 12.09 %. The measurement shown in the right figure denotes a duty cycle of 12.2 % which conforms with the calculated duty cycle. The small increase to the calculated value is due to losses in non-ideal components. According to the datasheet the switching frequency should be between 109 kHz and 137 kHz [28, p. 4]. This also conforms with the measured frequency of 123.9 kHz.

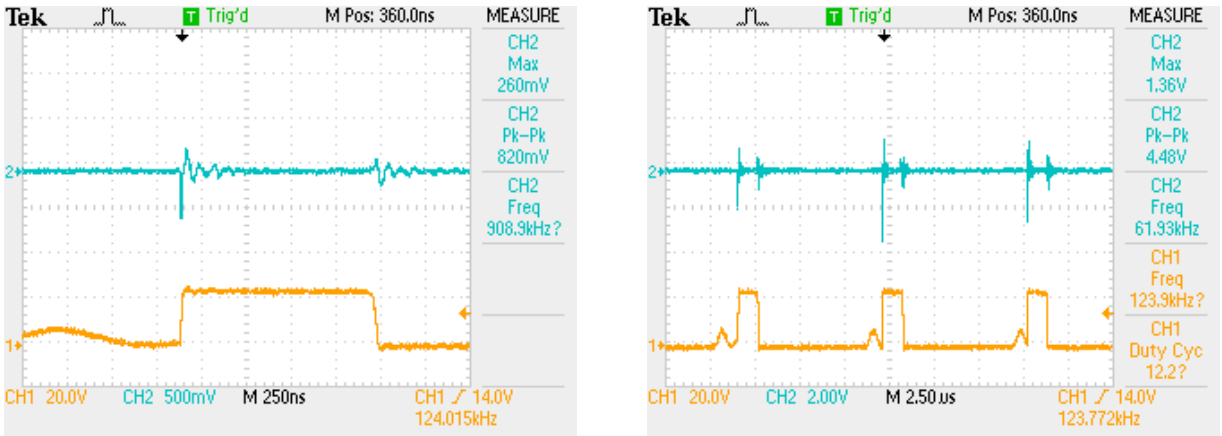

Figure 6.1.: Switch-node and output voltage of the 3.3 V switch-mode power supply.

Measurements on the output rails of all switch-mode power supply circuits present in the system show high frequency ringing when the inductor is switched on and off. This ringing can be observed at the ground plane of the system as well. This is due to the setup of the measurement system: the reference ground connection of the oscilloscope is connected directly to the lab power supply providing 24 V input voltage to the system under test. The oscilloscope therefore shows the difference between this distant

ground point and the output of the power supply circuits. Measuring the output rails using the ground plane on the tested boards itself as ground reference shows much less ringing.

Figure 6.2 shows measurements performed on the switch-mode power supply providing ±15 V and +5 V to the operational amplifiers located on the driver boards. The calculated duty cycle for this switch-mode power supply is 32.50 % which conforms to the measured duty cycle of 33.3 %. The calculated switching frequency of the implemented design is 254.902 kHz being slightly lower than the measured 280 kHz, but still in an acceptable range.

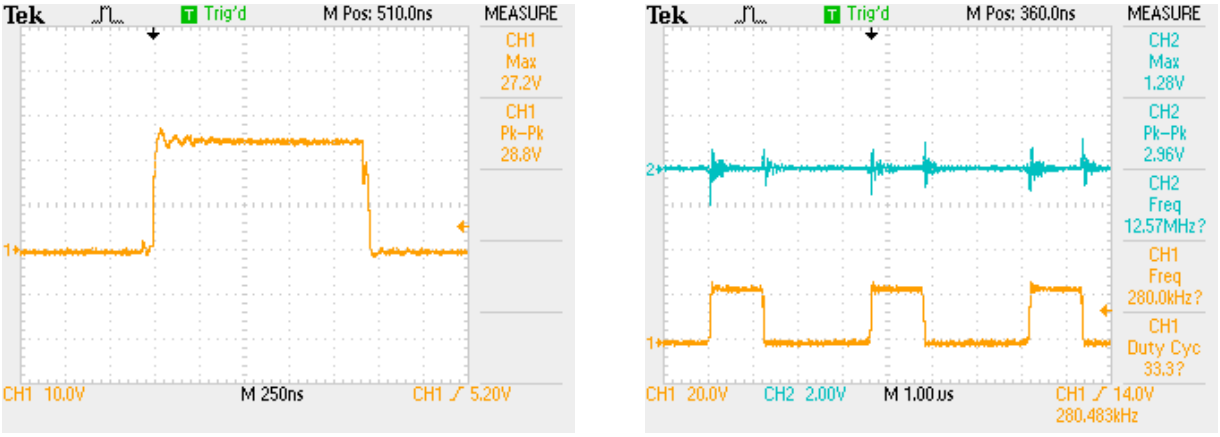

Figure 6.2.: Switch-node and +5 V output voltage of the ±15 V and +5 V switch-mode power supply.

Measurements on the high-voltage switch-mode power supply providing ±210 V to the system are shown in figure 6.3. The topology of this power supply is different from the two previously shown power supplies, because it controls an external N-channel MOSFFT as switching capacitor. The channel 1 probe and trigger in the measurements, shown in figure 6.3, are placed at the gate of this transistor. Calculated duty cycle for this setup is 28 % which roughly conforms to the measured signal. The nominal switching frequency of this power supply should be at 316.456 kHz which is also visible in the measured data.

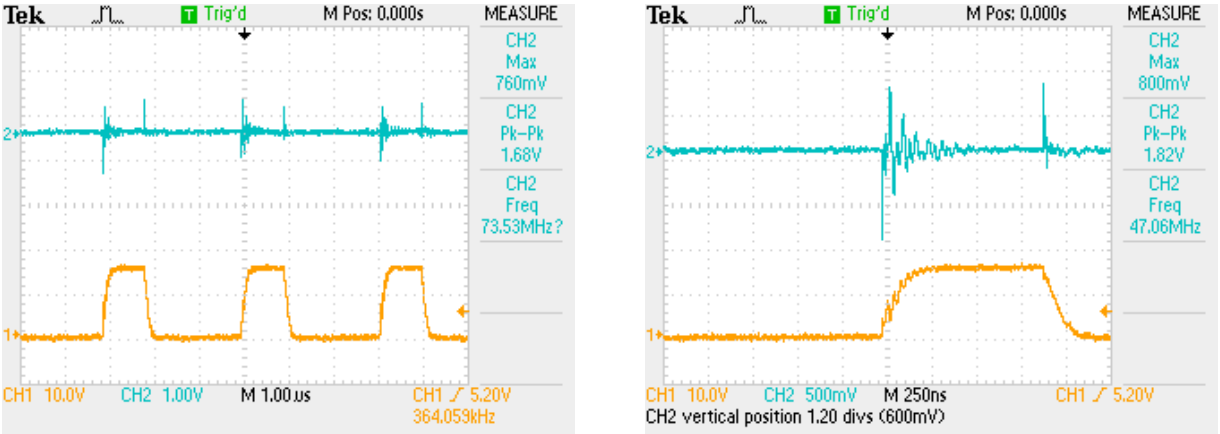

Figure 6.3.: Switch-node and noise on −210 V output voltage (left) and current sense pin (right) of the high-voltage switch-mode power supply.

The power supply blocks in the system provide the required voltages as designed and their behavior conforms to the calculations performed in the design phase of the system. Disregarding the high switching noise on the output voltages provided by the power supply blocks, it is visible that more power can be

provided by these circuit blocks than required by the blocks connected to their output. This becomes especially visible by the constant level of the output voltages independent from the point in time in regards to the switching cycle.

6.2 Signal Generation

Key characteristic of the designed system is the ability to provide the required signal with high quality at the output terminals of the driver board. The following measurements show the performance of the system under a variety of configuration parameters for the waveform generator block.

Figure 6.4 shows the performance of the system for all three base waveforms generated with the maximum gain factor of 121 (nominal) with the maximum required frequency of 5 kHz. The maximum vertical range of the utilized oscilloscope is 400 V. The measurements taken show that the peak-to-peak output voltage of the sine and square waves stays slightly below the maximum of 400 V. The triangular waveform shows an even greater degradation in the peak-to-peak voltage. The measurements also show that the part of the circuit driving the negative half wave is weaker than the part of the circuit driving the positive half wave. The shape of the output signal shows also greater differences from the waveform at the input of the system at the lower boundary of the output signal than at the upper boundary. The frequency of the generated signals is slightly lower than the target frequency of 5 kHz.

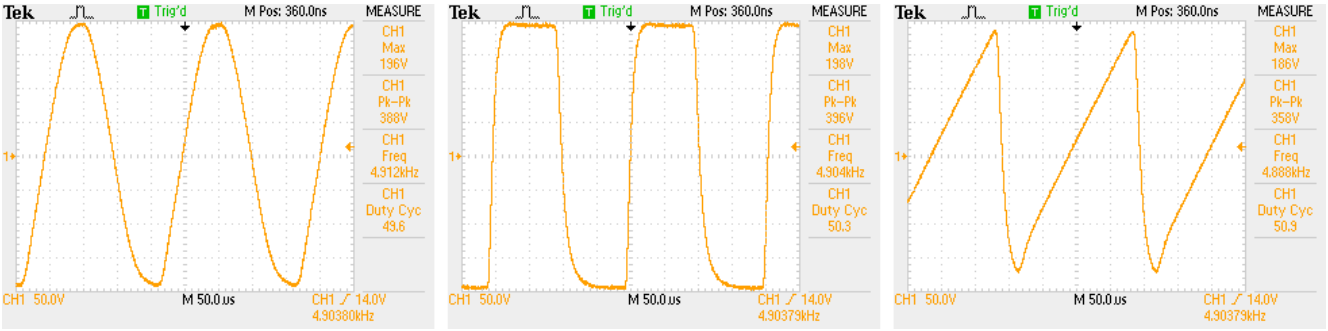

Figure 6.4.: Output with maximum gain of all three base waveforms.

The maximum gain of the system can be adjusted by changes in the resistor values of the feedback network of the operational amplifier. Therefore, an output voltage of ±200 V can be easily achieved with this small adjustment to the existing design. To improve the slope of the system, the value of the feedback capacitor connected between the output of the integrated operational amplifier and the positive input (C_{52}) can be decreased.

Figure 6.5 shows the other extreme of the output signal with minimum gain factor of 24.32 (nominal) and a minimum output frequency of 10 Hz. The nominal output voltage for these operating parameters should be 80.26 V. The measurements show that the actual output voltage is at 82 V slightly above the calculated value. In comparison to the previous measurements, it is notable that the shape of the generated waveforms matches almost exactly the optimum shape for each waveform type. The target output frequency of 10 Hz is also exactly matched.

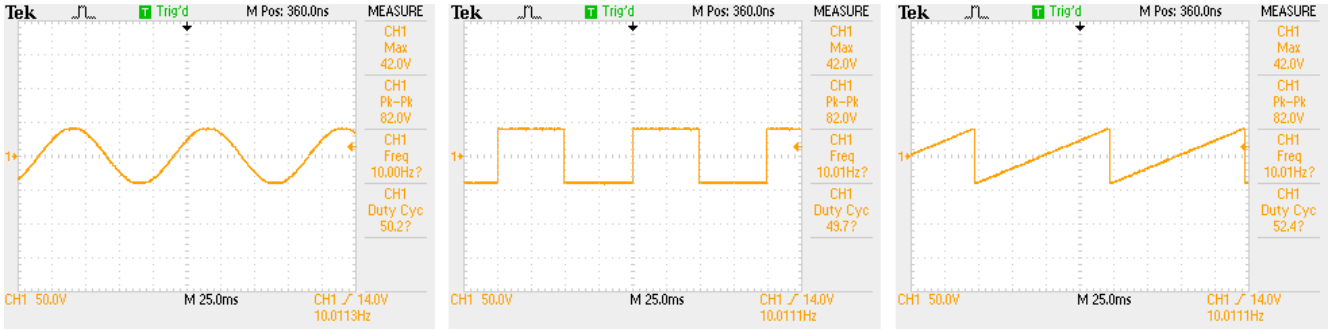

Figure 6.5.: Output with minimum gain of all three base waveforms.

To decrease the amplitude of the generated waveforms even more, the amplitude of the input signal to the amplifier circuit block needs to be decreased. This can be achieved by the *scale factor* operating parameter which scales the waveform embedded as template in the firmware before it is outputted using the DAC. For the measurements shown in the following figure a scale factor of 0.1 was applied to the template waveforms. This should yield a peak-to-peak voltage of 330 mV of the signal outputted by the DAC and a 8.03 V output peak-to-peak voltage of the system. The measurements shown in figure 6.6 have a peak-to-peak voltage of 8.56 V to 9.04 V not exactly matching the target value, but the principle operation of the waveform scaling parameter is visible. The configured output frequency for the measurements shown in figure 6.6 is 1 kHz.

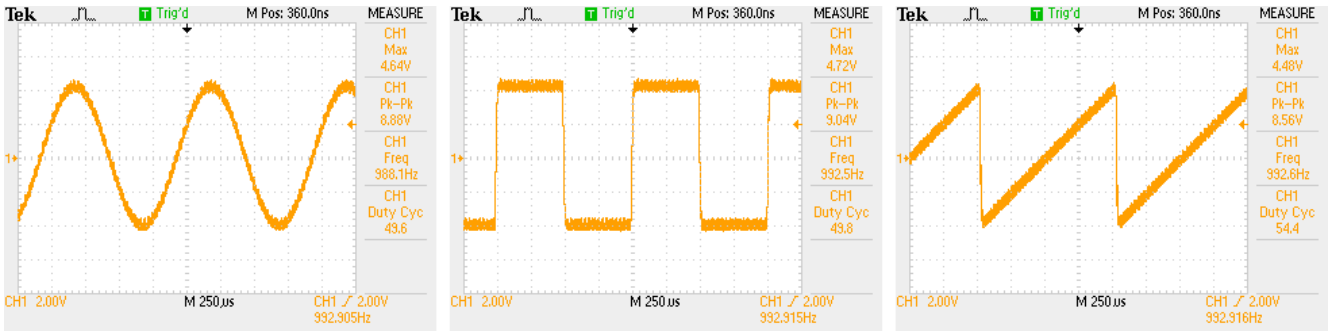

Figure 6.6.: Output with minimum gain of all three base waveforms scaled by factor of 0.1.

Due to the higher resolution per division in the measurements shown in figure 6.6, it is visible that the output signal contains superimposed noise on the generated waveform. This noise is clearly visible in figure 6.7 showing a measurement of the system output in idle mode with no generated waveform at the output.

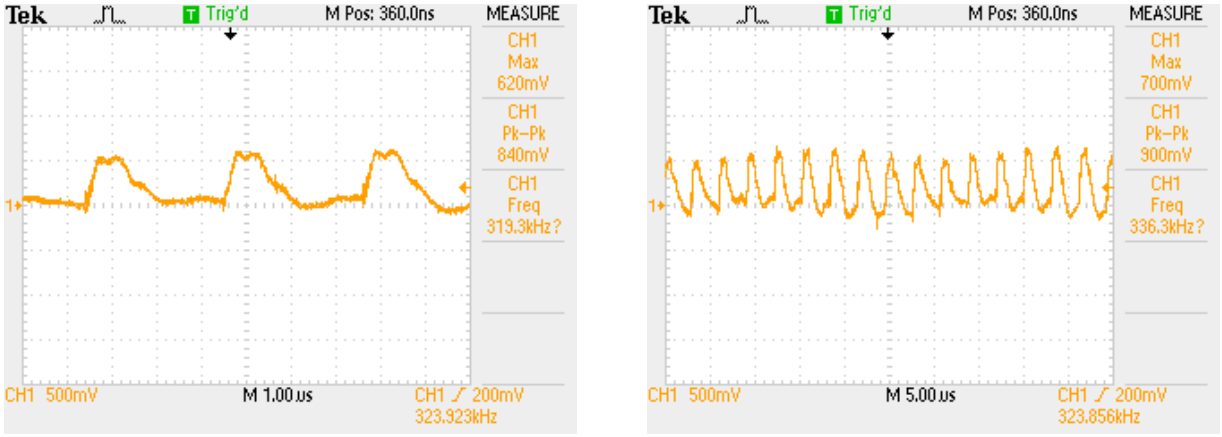

Figure 6.7.: Noise at the output of the system.

Reason for this noise at the output is a not perfectly stable output amplifier leading to continuous ringing and adjusting of the output by the integrated operational amplifier. Resolving this issue requires a closer examination of the amplifier stage build out of discrete transistors and the integrated operational amplifier. The measurement system itself interacts with the tested system which is revealed by a change in frequency and amplitude of the ringing depending on the number of probes connected to the output amplifier. Removing any influence of the measurement system on the observed behavior would require the use of active probes which are not available in the lab provided for the work done on this project.

All measurements were done with the EL device "*Probe 1398*" provided for testing purposes. This EL device has a capacitance of about 2.84 nF, a series resistance of about 1.40 kΩ and a resistance in parallel to the capacitive component of about 25.55 MΩ [3].

6.3 Power Consumption

A system consisting of one controller board and a single driver board has a power consumption of about 6.576 W. This corresponds to a current consumption of 274 mA for an input voltage of 24 V.

Table 6.1 shows the current consumption of a single driver board for all generated supply voltages required by the different sub-systems.

Table 6.1.: Current consumption grouped by supply voltages.

Supply Voltage	Current Consumption
3.3 V	20 mA
+15 V	51 mA
−15 V	−5.2 mA
+210 V	7.8 mA
−210 V	−6.0 mA

The current consumed by the controller board measured at the output of the 3.3 V switch-mode power supply is 68 mA.

The sum of all currents multiplied with their corresponding supply voltage yields a power consumption of all *consuming* circuit blocks of 4.03 W. Therefore, the power supply circuits have a power consumption of

2.54 W which corresponds to an efficiency of 61 %. The current consumption shown in table 6.1 and the measurements on the power supply blocks discussed in section 6.1 show that the power supplies were designed for supplying much higher currents. When operated in these higher power regions their efficiency would increase, because the power consumed by themselves does not increase linearly with the power drawn from the power supply blocks. An increased efficiency of the system when operated with lower power consumption can be achieved by adjusting the design for lower maximum output current.

6.4 Manufacturing Costs

One of the requirements set out for the design of the system discussed in the foregoing chapters is to stay within a budget of 150 to 200 euro per driver board. Table 6.2 shows the component and PCB manufacturing costs for the driver and controller boards calculated for a production quantity of 50 driver boards and 6 controller boards.

Table 6.2.: Component and PCB costs of the driver and controller boards.

Position	**Production Quantity**	**Costs / Euro**
Components for driver board	50	71.59
Driver board PCB	50	10.55
Components for controller board	6	57.19
Controller board PCB	6	20.98

Summing up the numbers in table 6.2 yields total costs for a single driver board of 82.14 euro and 78.17 euro for a single controller board. Splitting the costs for 6 controller boards results in average costs of 91.52 euro for a single driver board.

7 Conclusion and Outlook

This thesis discusses the design and implementation of a driver circuit for the excitation of electroluminescent devices. Preceding to the design and implementation of the selected architecture to meet the set requirements, various other approaches were evaluated and are discussed in the respective chapter. To reach the final design incorporating all aspects deducted from the specified requirements and fulfilling the goals set on project start, multiple power supply, analog, and digital circuits had to be designed as well as two communication protocols and software running as firmware on two microcontrollers.

The resulting design meets the requirements and is able to drive electroluminescent devices with various operating parameters, but is also limited in accuracy and is therefore not well suited to be used as a signal generator for other, general applications requiring the generation of arbitrary waveforms with high output voltages. The limits of the designed system are acceptable in the context of the contemplated application to drive electroluminescent devices, because a high waveform accuracy is not required and the trade-offs in accuracy do not carry weight.

Although the design of the system is complete and meeting the requirements, various aspects could be improved by further investigations of the hardware design. Points of improvement include the stability of the operational amplifier block, the efficiency of power supply circuits and further protection against faulty operation. The software deployed as firmware on the two microcontrollers enables control of all necessary parameters to use the system as intended, but also allows a multitude of further extensions. The hardware design already contains additional features not leveraged by software yet, like the non-volatile EEPROM memory for storage of operating parameters and the current sense amplifier block to conduct measurements on the load connected to the system. Other extensions could be incorporated to improve the stability and usability of the system.

Beside the scientific task to design a system for the given requirements, the implementation and a focus on the possibility to manufacture the resulting system in a short run, for usage in further scientific projects were a major part of the work done in this project. The presented design with all implementation details combines both aspects.

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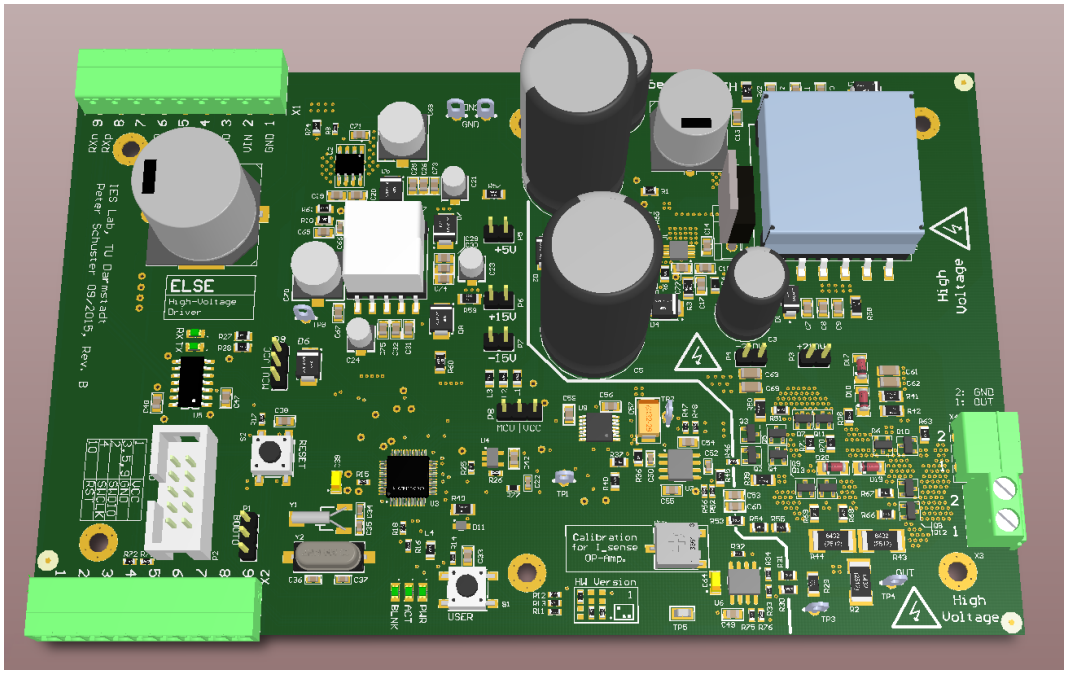
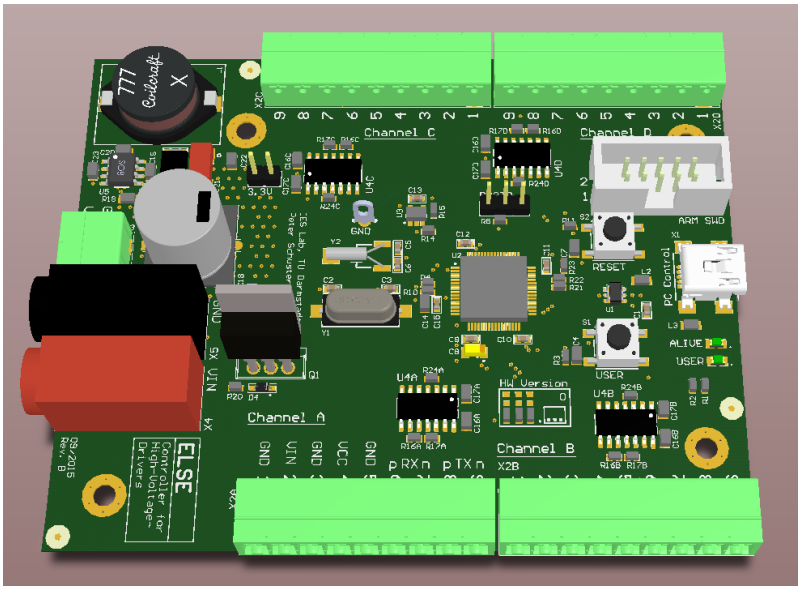
B Appendix

B.1 3D Renderings

B.1.1 Driver Board

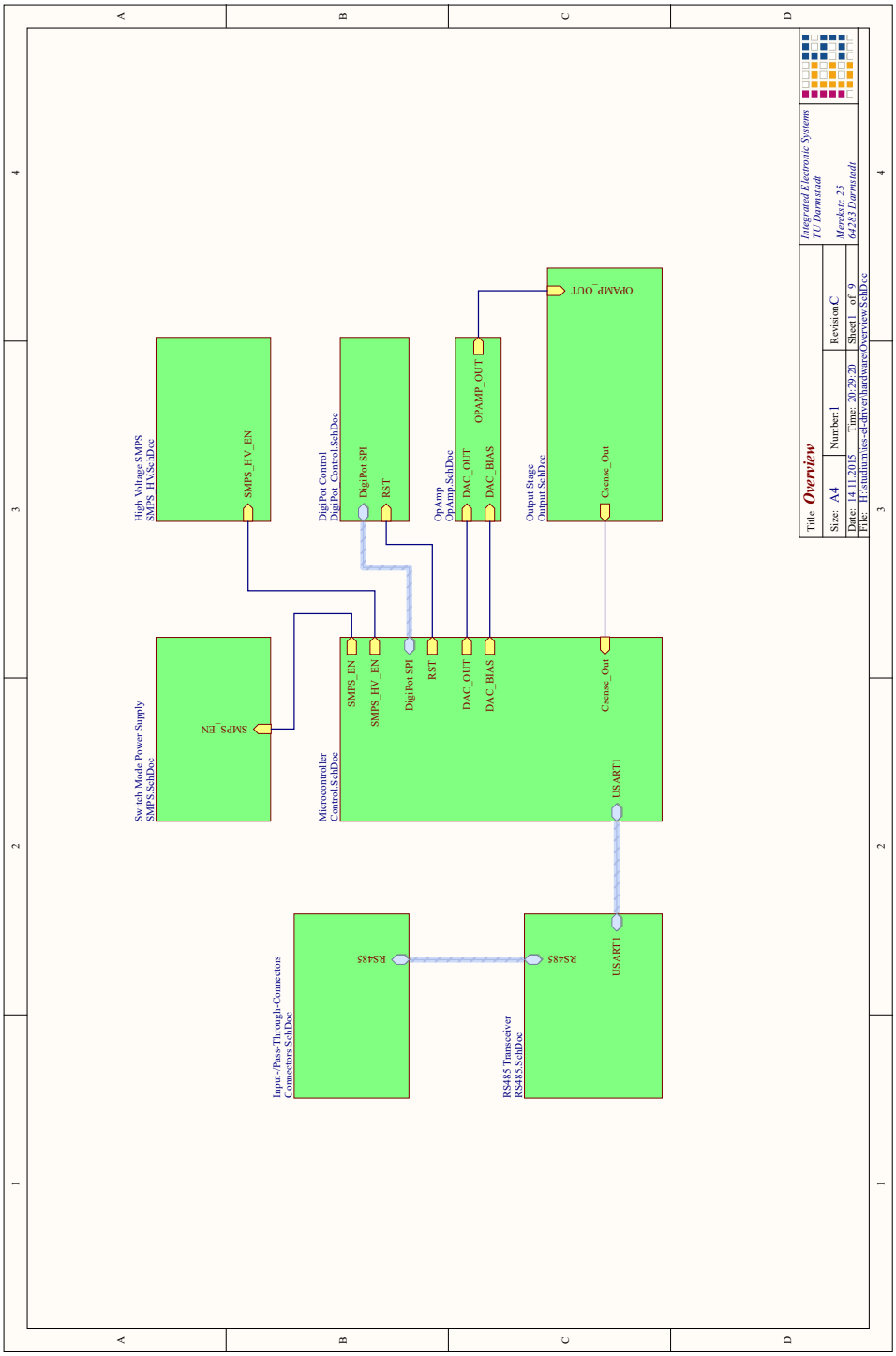


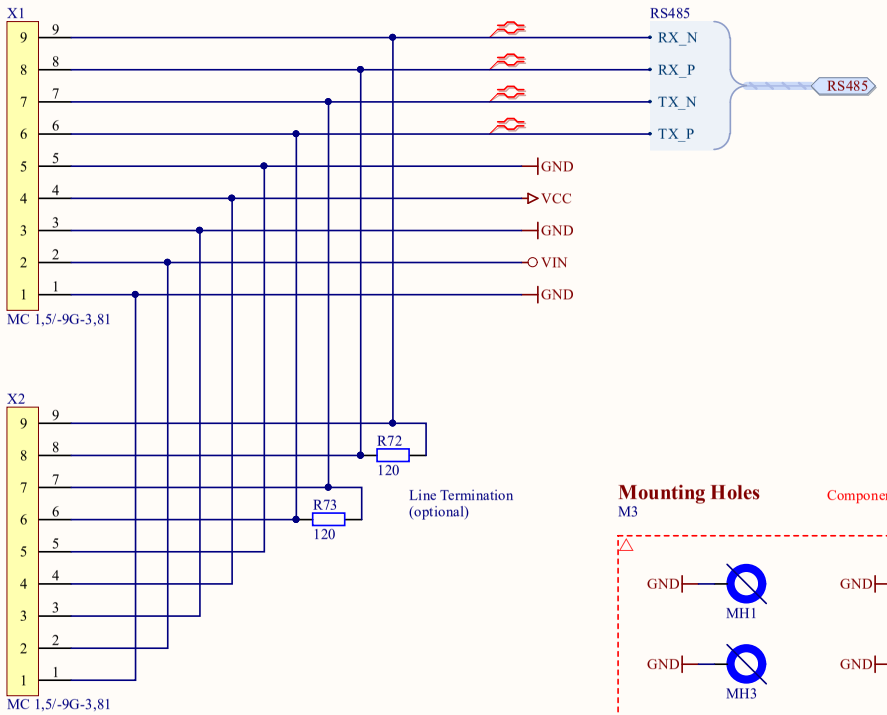
B.1.2 Controller Board



B.2 Schematics

B.2.1 Driver Board





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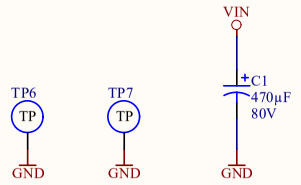
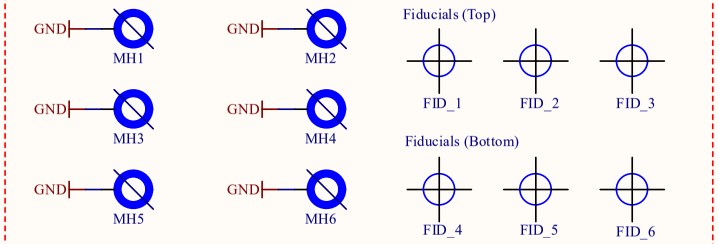


Mounting Holes

M3

Component Class: "Mechanical"



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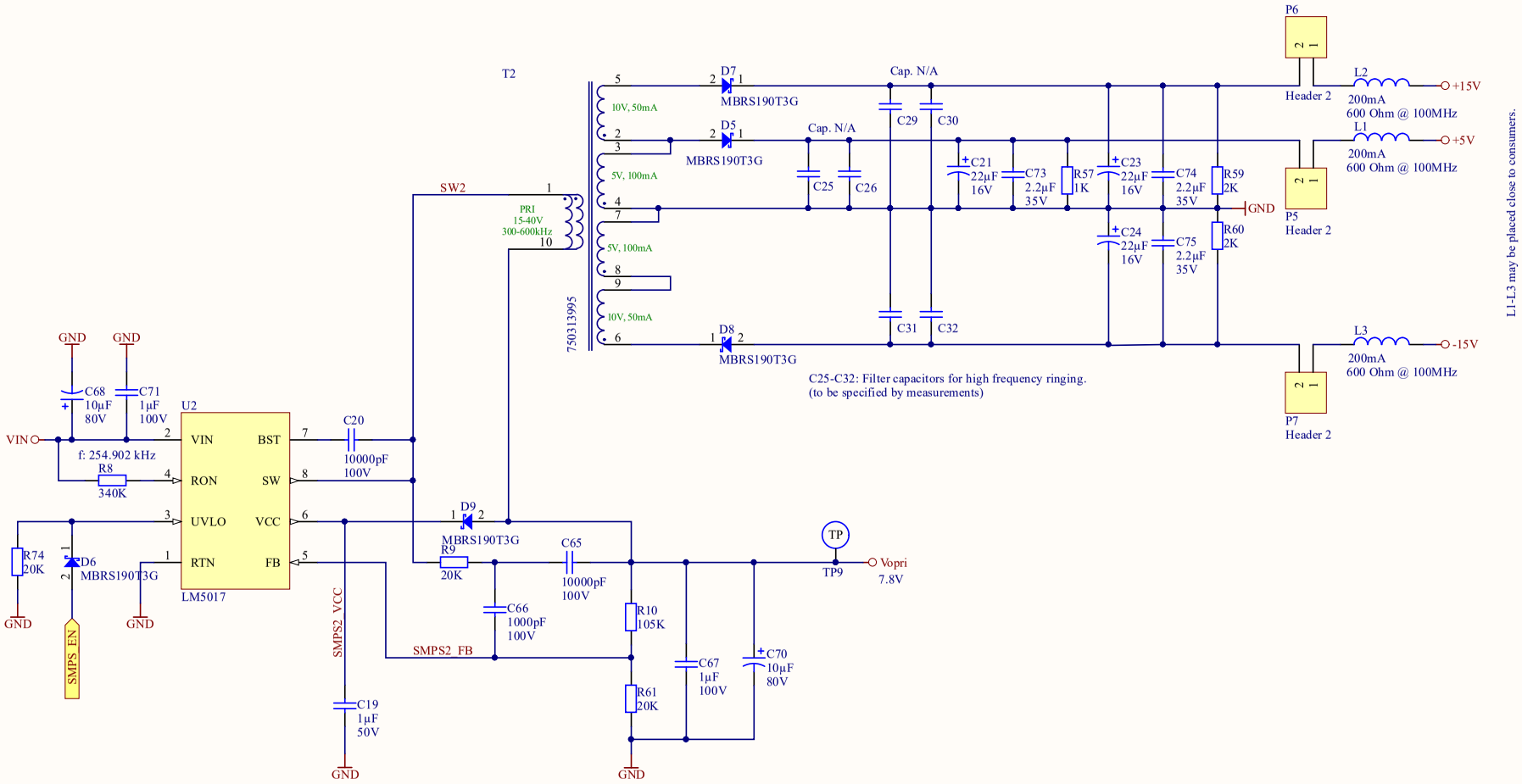

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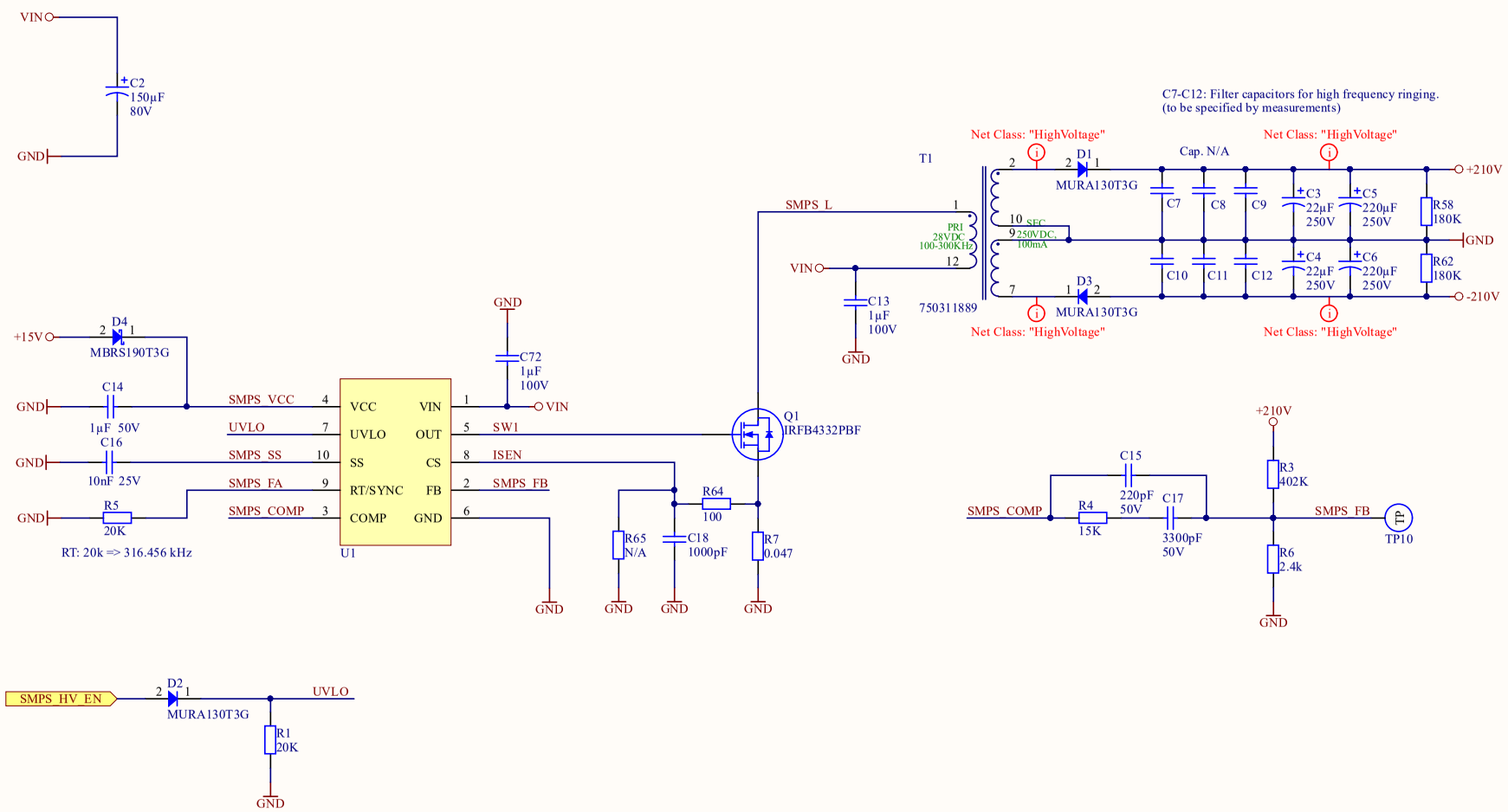
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80V
GND
C7-C12: Filter capacitors for high frequency ringing.
(to be specified by measurements)
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Net Class: "HighVoltage"
T1
Cap. N/A
D1
MURA130T3G
+210V
SMPS_L
PRI
28VDC
100-300KHz
SEC
250VDC,
100mA
C7
C8
C9
C3
22µF
250V
C5
220µF
250V
R58
180K
GND
VIN
C10
C11
C12
C4
22µF
250V
C6
220µF
250V
R62
180K
C13
1µF
100V
750311889
D3
MURA130T3G
-210V
Net Class: "HighVoltage"
Net Class: "HighVoltage"
GND
+15V
D4
MBRS190T3G
C14
1µF 50V
GND
C16
10nF 25V
GND
R5
20K
GND
RT: 20k => 316.456 kHz
SMPS_VCC
UVLO
SMPS_SS
SMPS_FA
SMPS_COMP
VCC
UVLO
SS
RT/SYNC
COMP
VIN
OUT
CS
FB
GND
U1
C72
1µF
100V
VIN
SW1
ISEN
SMPS_FB
Q1
IRFB4332PBF
R64
100
R65
N/A
C18
1000pF
R7
0.047
GND
GND
GND
GND
+210V
C15
220pF
50V
SMPS_COMP
R4
15K
C17
3300pF
50V
R3
402K
SMPS_FB
TP
TP10
R6
2.4k
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SMPS_HV_EN
D2
MURA130T3G
UVLO
R1
20K
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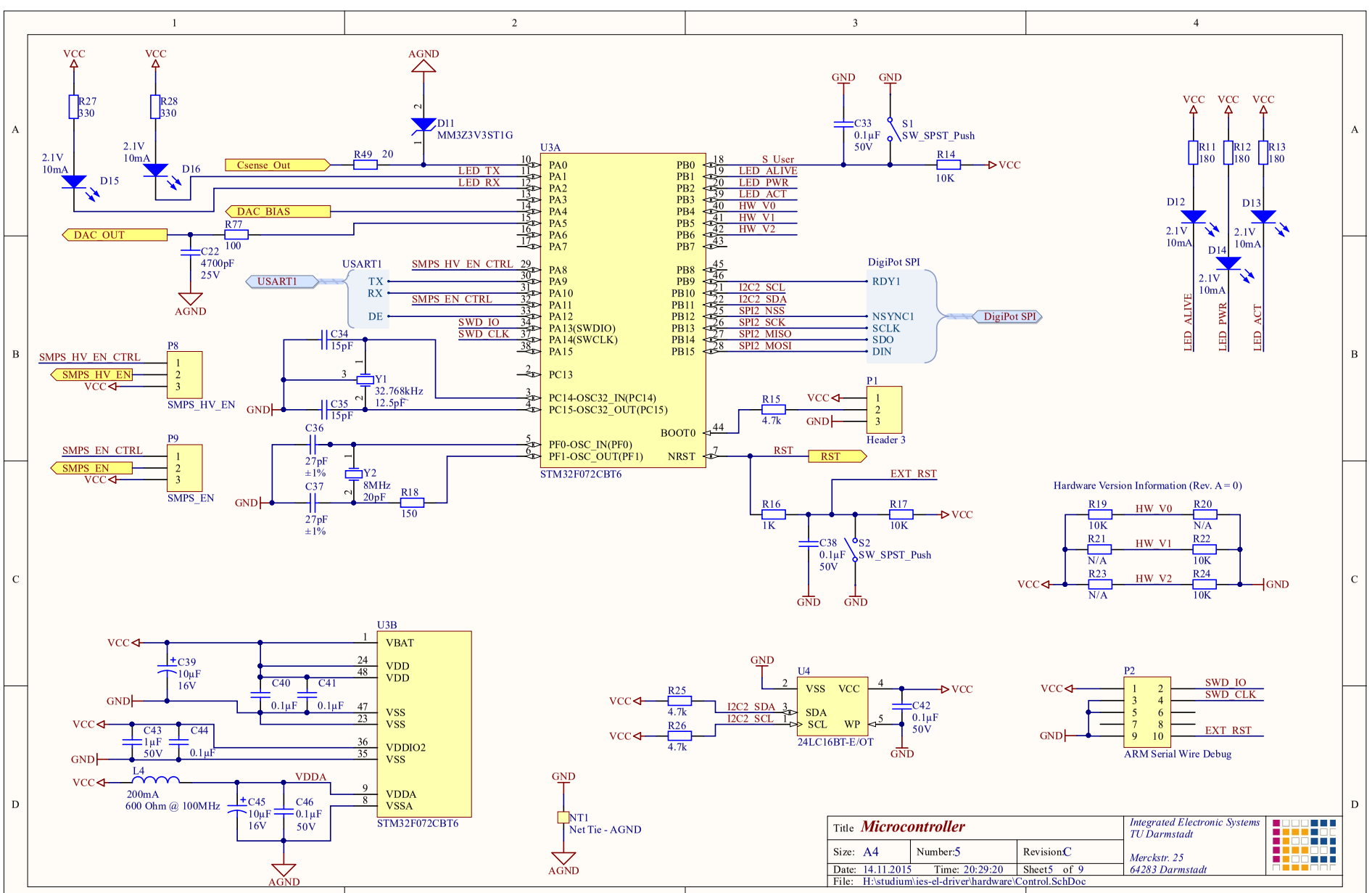
TU Darmstadt
Merckstr. 25
64283 Darmstadt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R28 330
2.1V 10mA
D15
D16
AGND
D11 MM3Z3V3ST1G
Csense_Out
R49 20
DAC_BIAS
DAC_OUT
R77 100
C22 4700pF 25V
U3A
STM32F072CBT6
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PA8
PA9
PA10
PA11
PA12
PA13(SWDIO)
PA14(SWCLK)
PA15
PC13
PC14-OSC32_IN(PC14)
PC15-OSC32_OUT(PC15)
PF0-OSC_IN(PF0)
PF1-OSC_OUT(PF1)
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PB8
PB9
PB10
PB11
PB12
PB13
PB14
PB15
BOOT0
NRST
LED_TX
LED_RX
USART1
SMPS_HV_EN_CTRL
SMPS_EN_CTRL
SWD_IO
SWD_CLK
S_User
LED_ALIVE
LED_PWR
LED_ACT
HW_V0
HW_V1
HW_V2
I2C2_SCL
I2C2_SDA
SPI2_NSS
SPI2_SCK
SPI2_MISO
SPI2_MOSI
RDY1
NSYNC1
SCLK
SDO
DIN
DigiPot SPI
C33 0.1µF 50V
S1 SW_SPST_Push
R14 10K
R11 180
R12 180
R13 180
D12
D13
D14
P8
P9
P1
Header 3
C34 15pF
C35 15pF
Y1 32.768kHz 12.5pF
C36 27pF ±1%
C37 27pF ±1%
Y2 8MHz 20pF
R18 150
R15 4.7k
R16 1K
R17 10K
RST
EXT_RST
C38 0.1µF 50V
S2 SW_SPST_Push
Hardware Version Information (Rev. A = 0)
R19 10K
R20 N/A
R21 N/A
R22 10K
R23 N/A
R24 10K
U3B
VBAT
VDD
VSS
VDDIO2
VDDA
VSSA
C39 10µF 16V
C40 0.1µF
C41 0.1µF
C43 1µF 50V
C44 0.1µF
L4 200mA 600 Ohm @ 100MHz
C45 10µF 16V
C46 0.1µF 50V
U4
24LC16BT-E/OT
VSS
VCC
SDA
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WP
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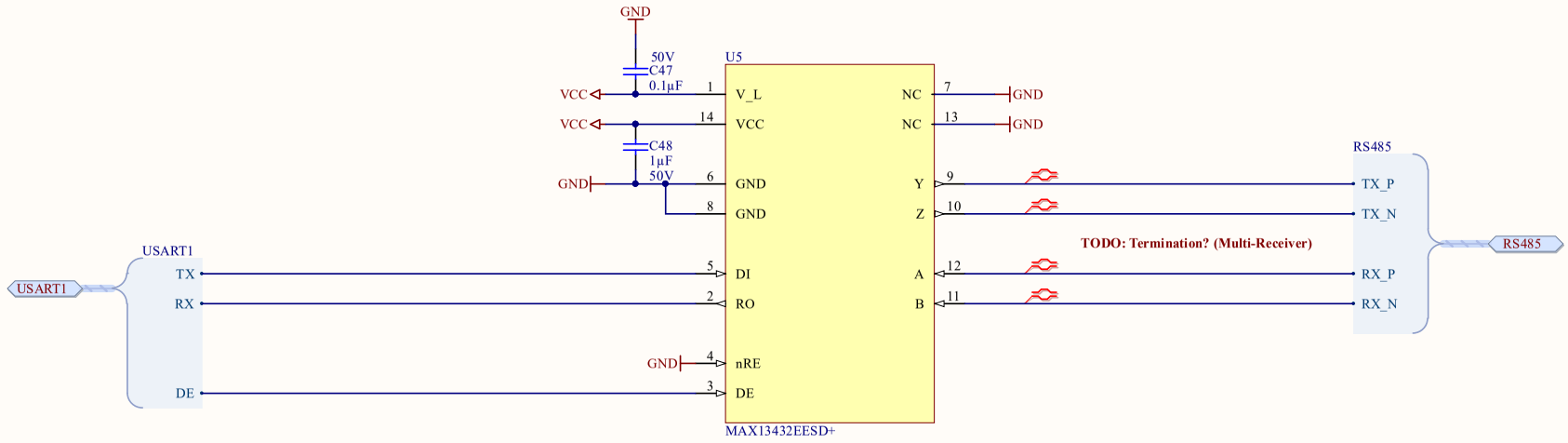
TU Darmstadt
Merckstr. 25
64283 Darmstadt



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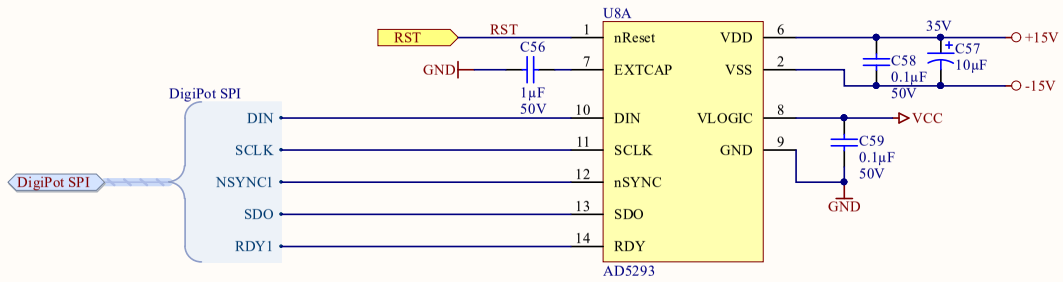

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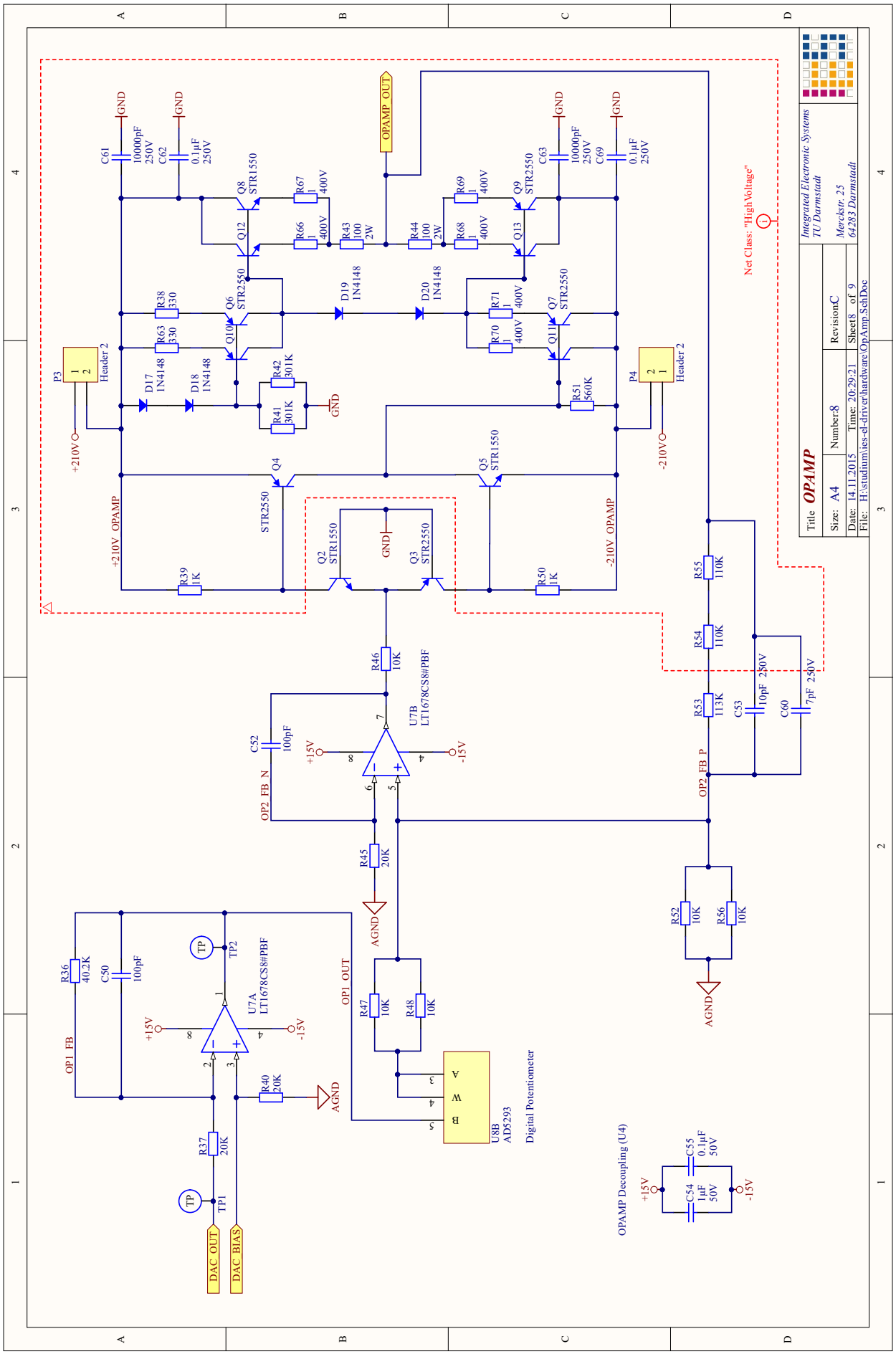
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TU Darmstadt
Merckstr. 25
64283 Darmstadt
Net Class: "HighVoltage"
OPAMP_OUT
+210V_OPAMP
-210V_OPAMP
+210V
-210V
OP2_FB_N
OP2_FB_P
OP1_FB
OP1_OUT
DAC_OUT
DAC_BIAS
AGND
GND
+15V
-15V
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Digital Potentiometer
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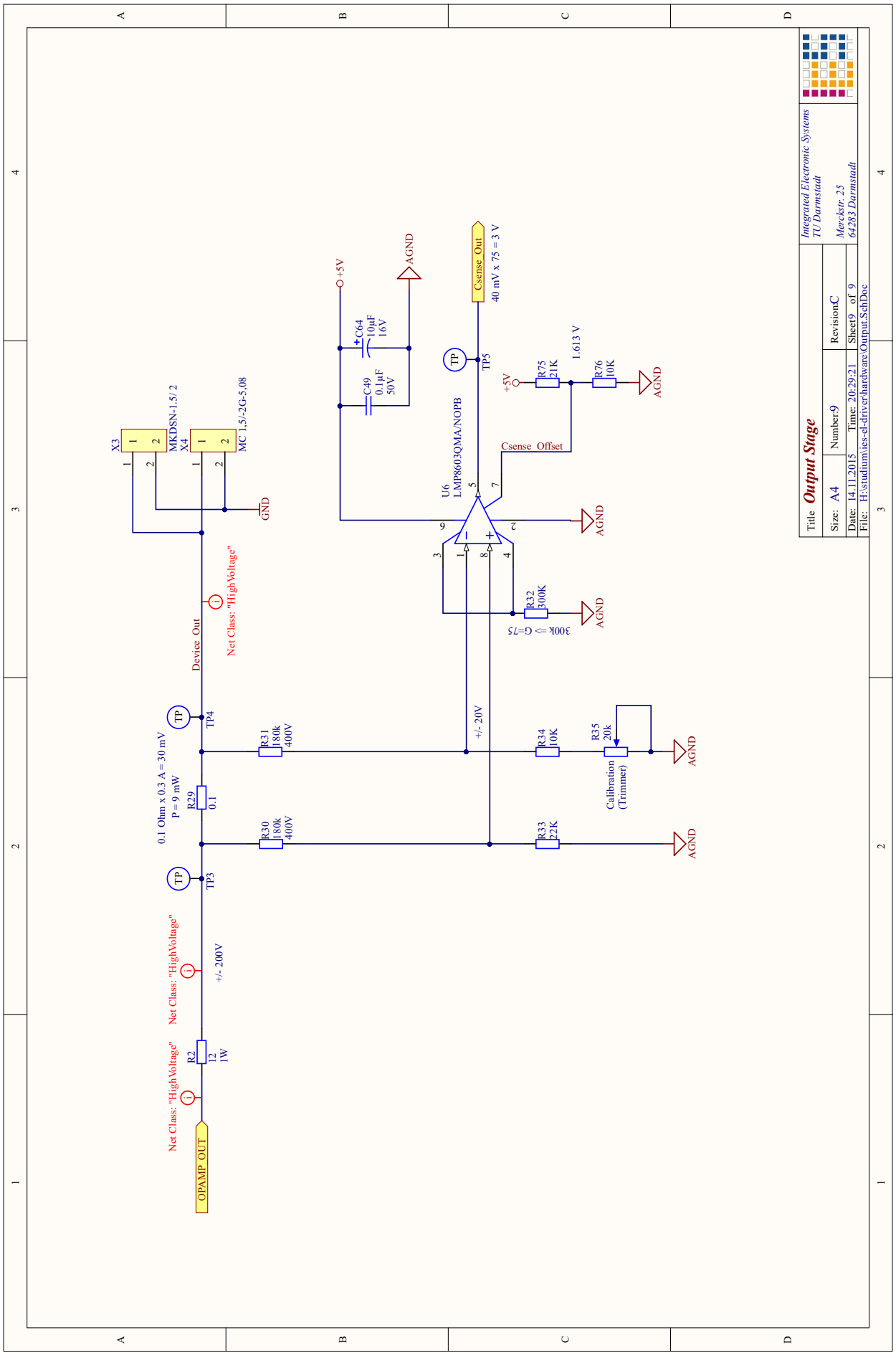
U7B LT1678CS8#PBF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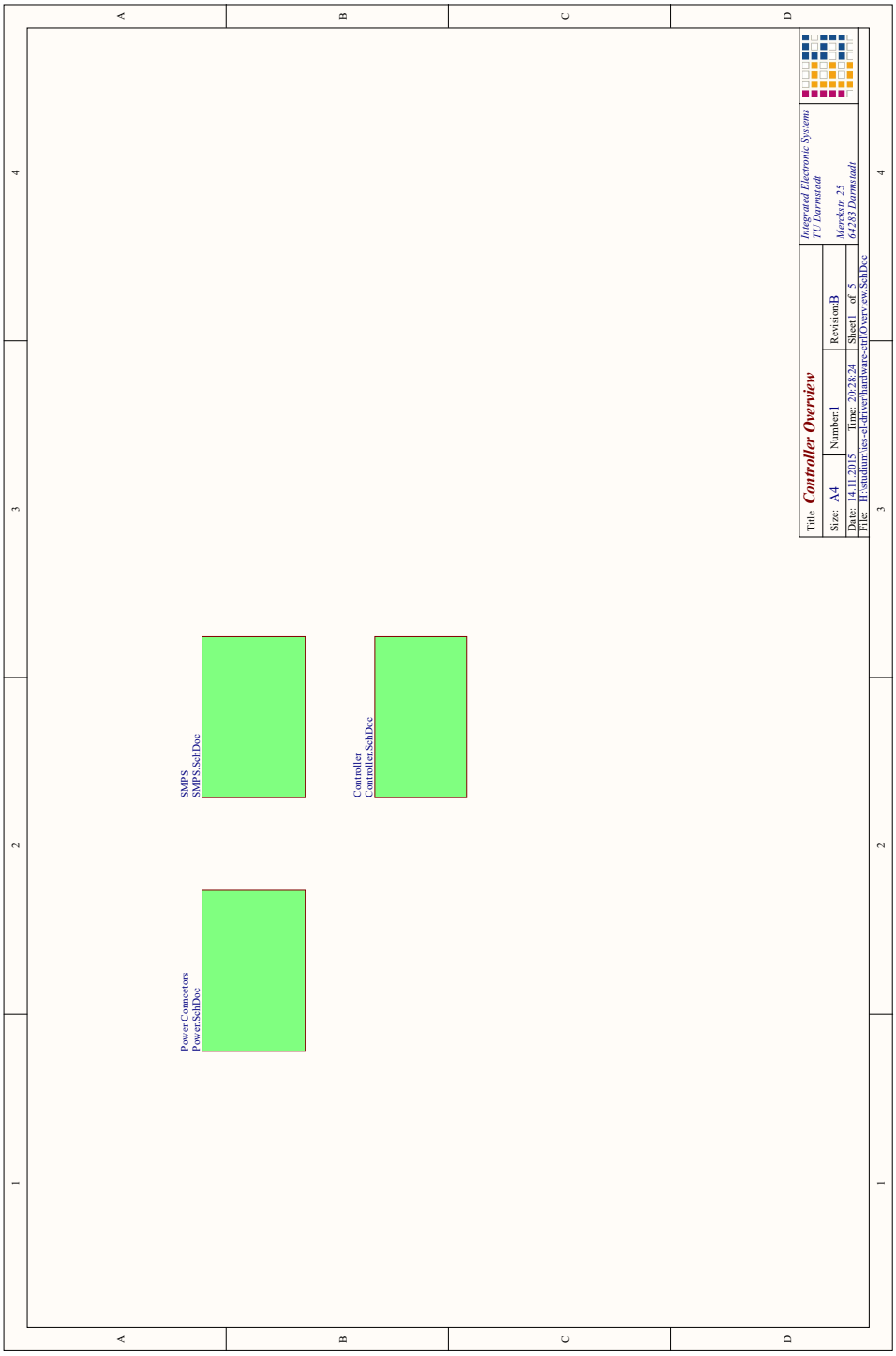
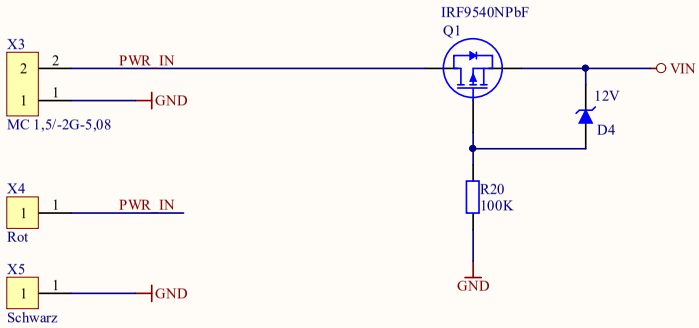
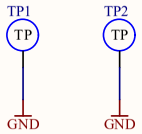
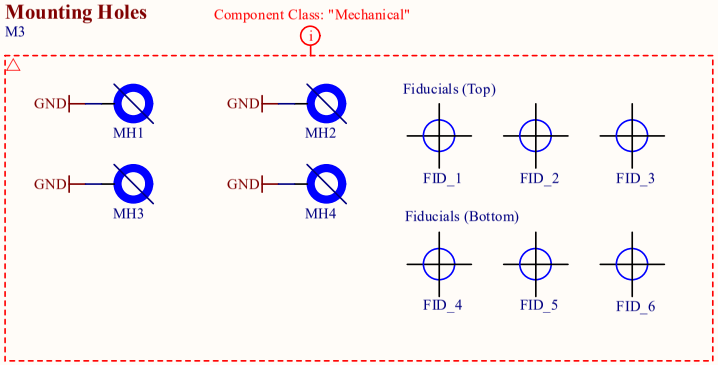
Integrated Electronic Systems
TU Darmstadt
Merckstr. 25
64283 Darmstadt
OPAMP OUT
Net Class: "HighVoltage"
R2
12
1W
+/- 200V
TP3
R29
0.1
0.1 Ohm x 0.3 A = 30 mV
P = 9 mW
R30
180k
400V
R33
22K
TP4
Device Out
R31
180k
400V
R34
10K
R35
20k
Calibration
(Trimmer)
AGND
+/- 20V
X3
MKDSN-1.5/ 2
X4
MC 1,5/-2G-5,08
GND
C49
0.1µF
50V
C64
10µF
16V
+5V
U6
LMP8603QMA/NOPB
R32
300K
300K => G=75
TP5
Csense Out
40 mV x 75 = 3 V
Csense Offset
R75
21K
R76
10K
1.613 V

B.2.2 Controller Board









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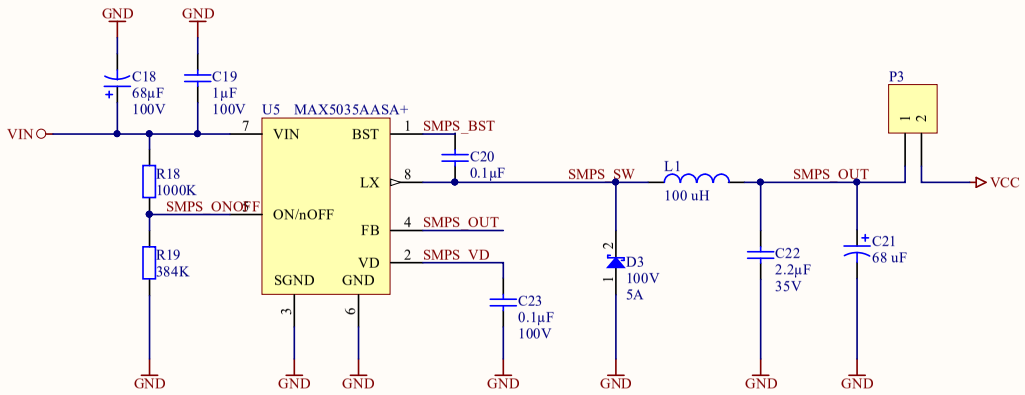

Title *SMPS [3.3V]*			*Integrated Electronic Systems TU Darmstadt*
Size: A4	Number:3	Revision:B	*Merckstr. 25 64283 Darmstadt*
Date: 14.11.2015 Time: 20:28:24		Sheet3 of 5	
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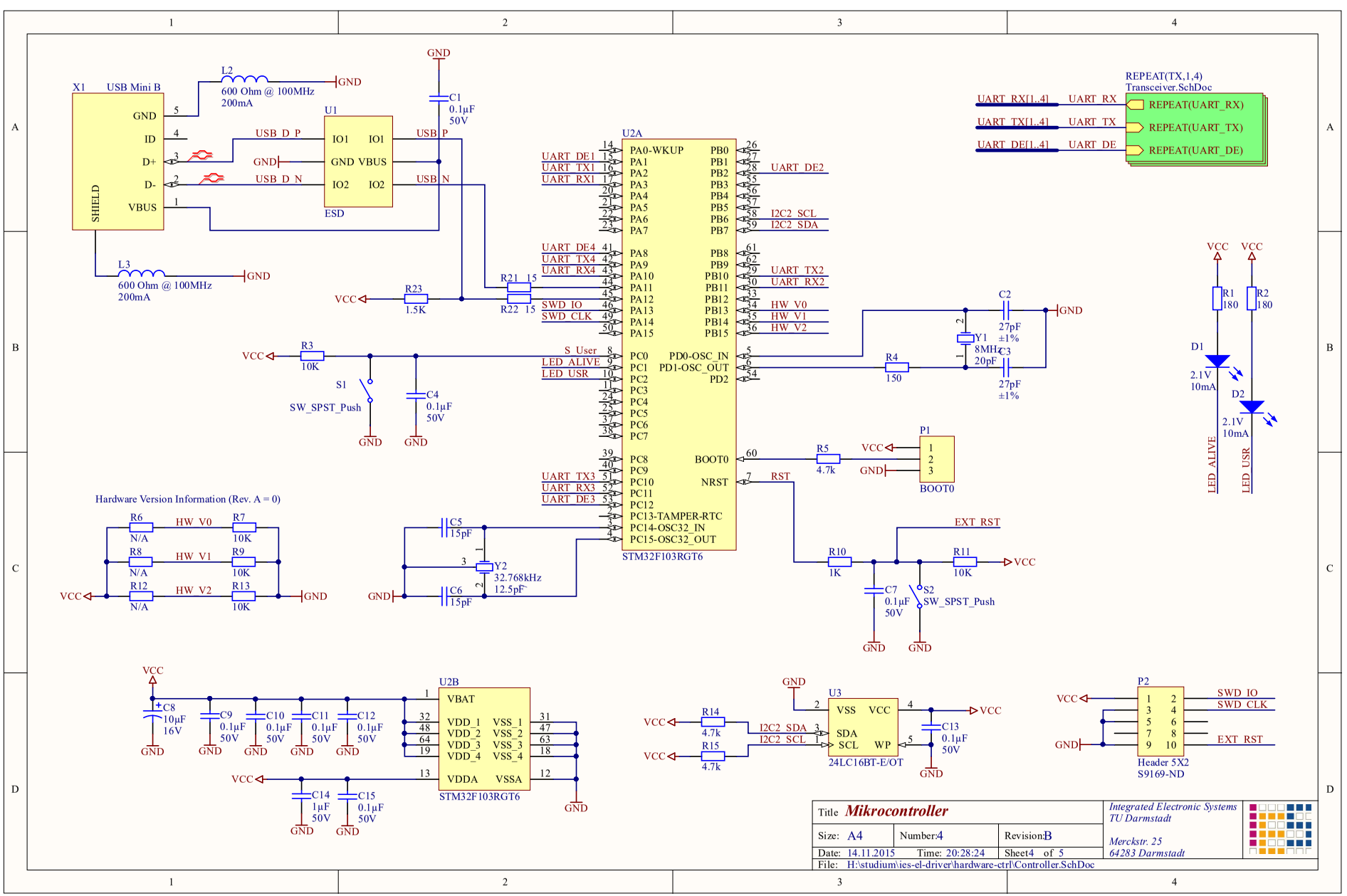
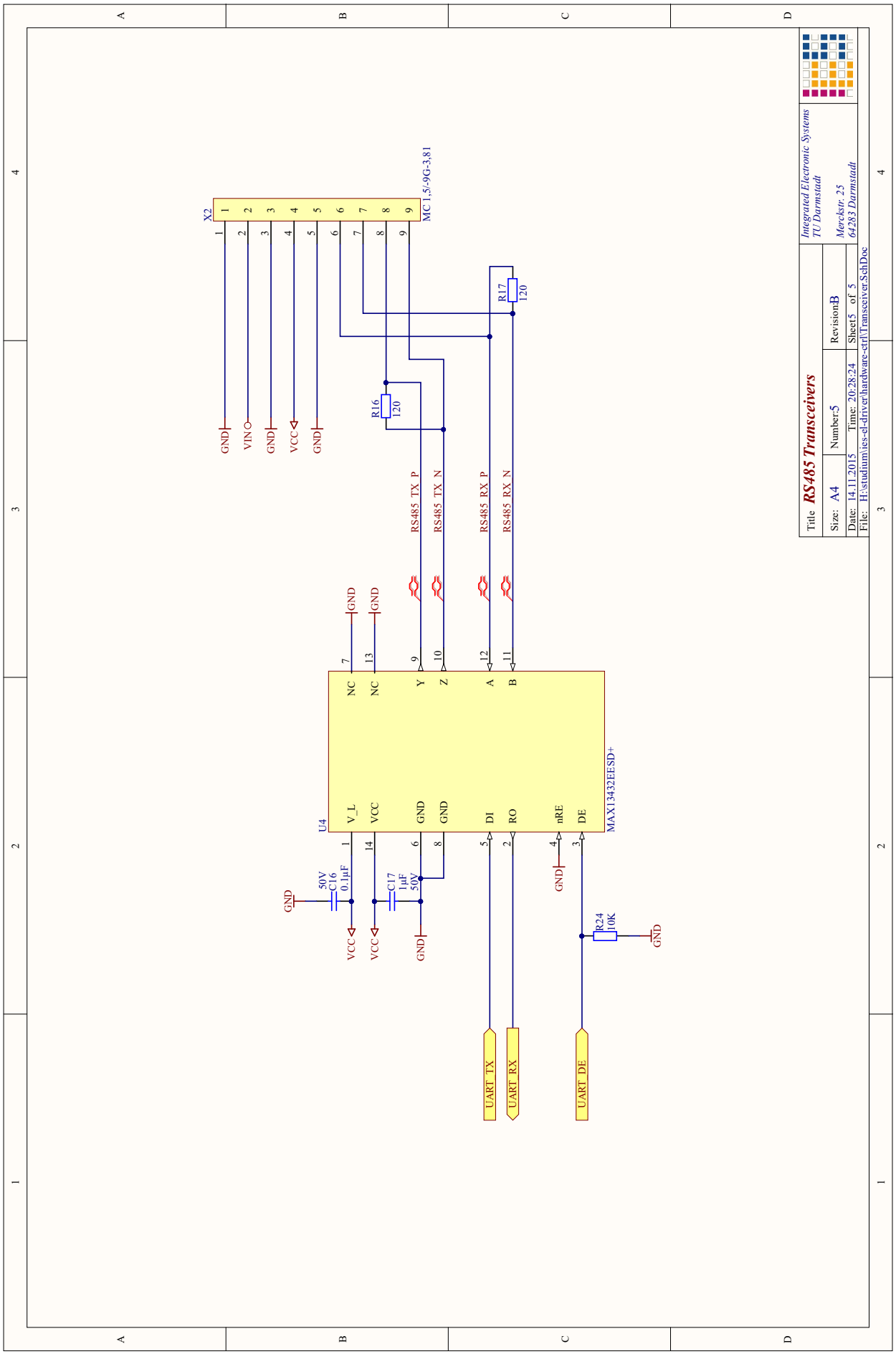
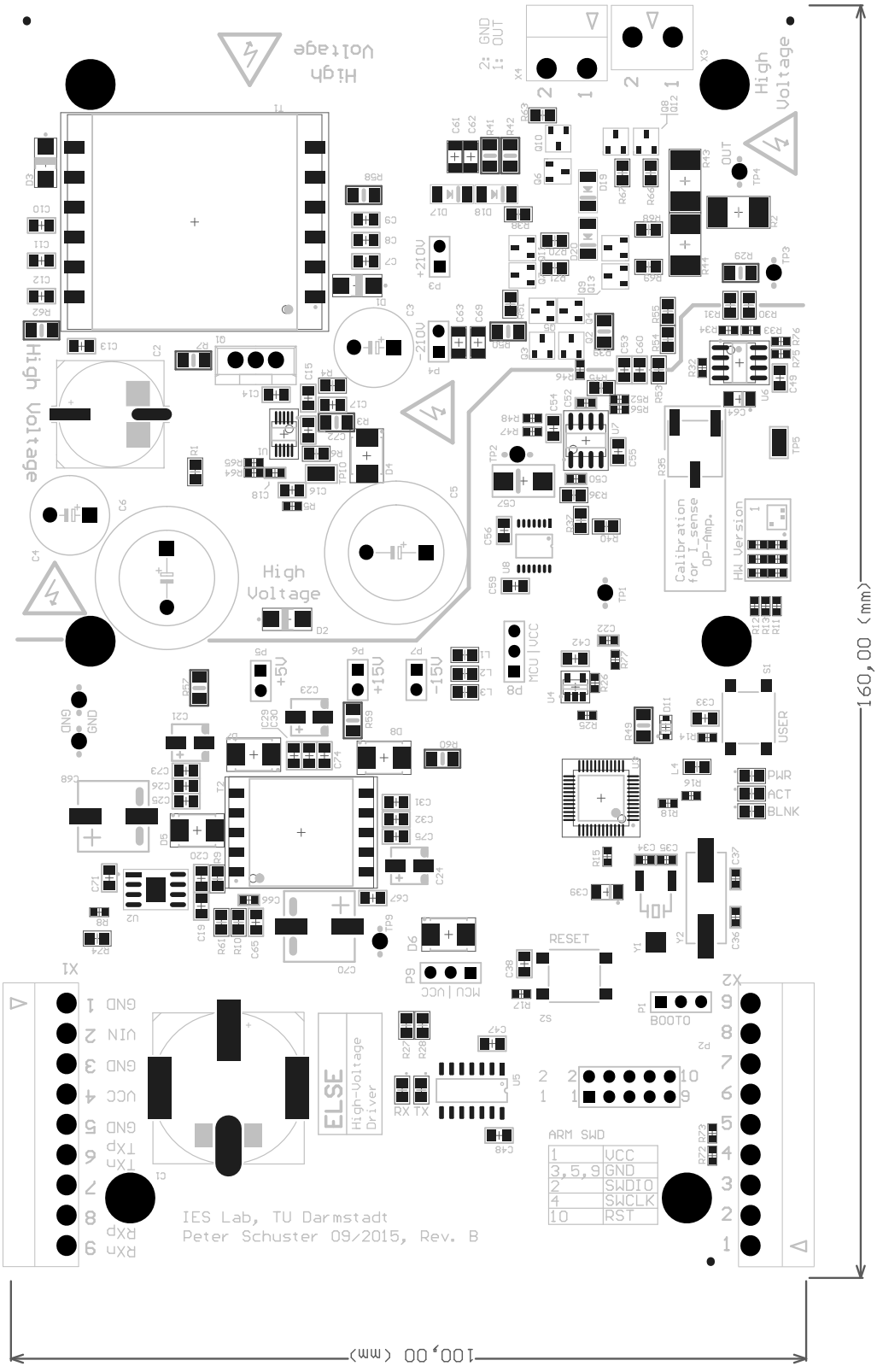

X1 USB Mini B
SHIELD
GND
ID
D+
D-
VBUS
L2
600 Ohm @ 100MHz
200mA
L3
600 Ohm @ 100MHz
200mA
U1
ESD
USB_D_P
USB_D_N
USB_P
USB_N
C1
0.1µF
50V
R23
1.5K
R21_15
R22_15
U2A
STM32F103RGT6
UART_DE1
UART_TX1
UART_RX1
UART_DE2
I2C2_SCL
I2C2_SDA
UART_DE4
UART_TX4
UART_RX4
UART_TX2
UART_RX2
SWD_IO
SWD_CLK
HW_V0
HW_V1
HW_V2
S_User
LED_ALIVE
LED_USR
UART_TX3
UART_RX3
UART_DE3
BOOT0
NRST
RST
PD0-OSC_IN
PD1-OSC_OUT
PC13-TAMPER-RTC
PC14-OSC32_IN
PC15-OSC32_OUT
R3
10K
S1
SW_SPST_Push
C4
0.1µF
50V
C2
27pF
±1%
Y1
8MHz
C3
20pF
27pF
±1%
R4
150
R5
4.7k
P1
BOOT0
R10
1K
R11
10K
EXT_RST
C7
0.1µF
50V
S2
SW_SPST_Push
Hardware Version Information (Rev. A = 0)
R6
N/A
R7
10K
R8
N/A
R9
10K
R12
N/A
R13
10K
C5
15pF
C6
15pF
Y2
32.768kHz
12.5pF
REPEAT(TX,1,4)
Transceiver.SchDoc
UART_RX[1..4]
UART_TX[1..4]
UART_DE[1..4]
REPEAT(UART_RX)
REPEAT(UART_TX)
REPEAT(UART_DE)
R1
180
R2
180
D1
2.1V
10mA
D2
2.1V
10mA
LED_ALIVE
LED_USR
C8
10µF
16V
C9
0.1µF
50V
C10
0.1µF
50V
C11
0.1µF
50V
C12
0.1µF
50V
U2B
VBAT
VDD_1
VDD_2
VDD_3
VDD_4
VSS_1
VSS_2
VSS_3
VSS_4
VDDA
VSSA
STM32F103RGT6
C14
1µF
50V
C15
0.1µF
50V
R14
4.7k
R15
4.7k
U3
24LC16BT-E/OT
VSS
VCC
SDA
SCL
WP
C13
0.1µF
50V
P2
Header 5X2
S9169-ND
Title Mikrocontroller
Size: A4
Number:4
Revision:B
Date: 14.11.2015
Time: 20:28:24
Sheet4 of 5
File: H:\studium\ies-el-driver\hardware-ctrl\Controller.SchDoc
Integrated Electronic Systems
TU Darmstadt
Merckstr. 25
64283 Darmstadt


X2
MC 1,5/-9G-3,81
GND
VIN
GND
VCC
GND
R16
120
R17
120
RS485_TX_P
RS485_TX_N
RS485_RX_P
RS485_RX_N
U4
MAX13432EESD+
V_L
VCC
GND
GND
NC
NC
Y
Z
A
B
DI
RO
nRE
DE
C16
0.1µF
50V
C17
1µF
50V
R24
10K
UART_TX
UART_RX
UART_DE
Title RS485 Transceivers
Size: A4
Number:5
RevisionB
Date: 14.11.2015
Time: 20:28:24
Sheet5 of 5
File: H:\studium\ies-el-driver\hardware-ctrl\Transceiver.SchDoc
Integrated Electronic Systems
TU Darmstadt
Merckstr. 25
64283 Darmstadt

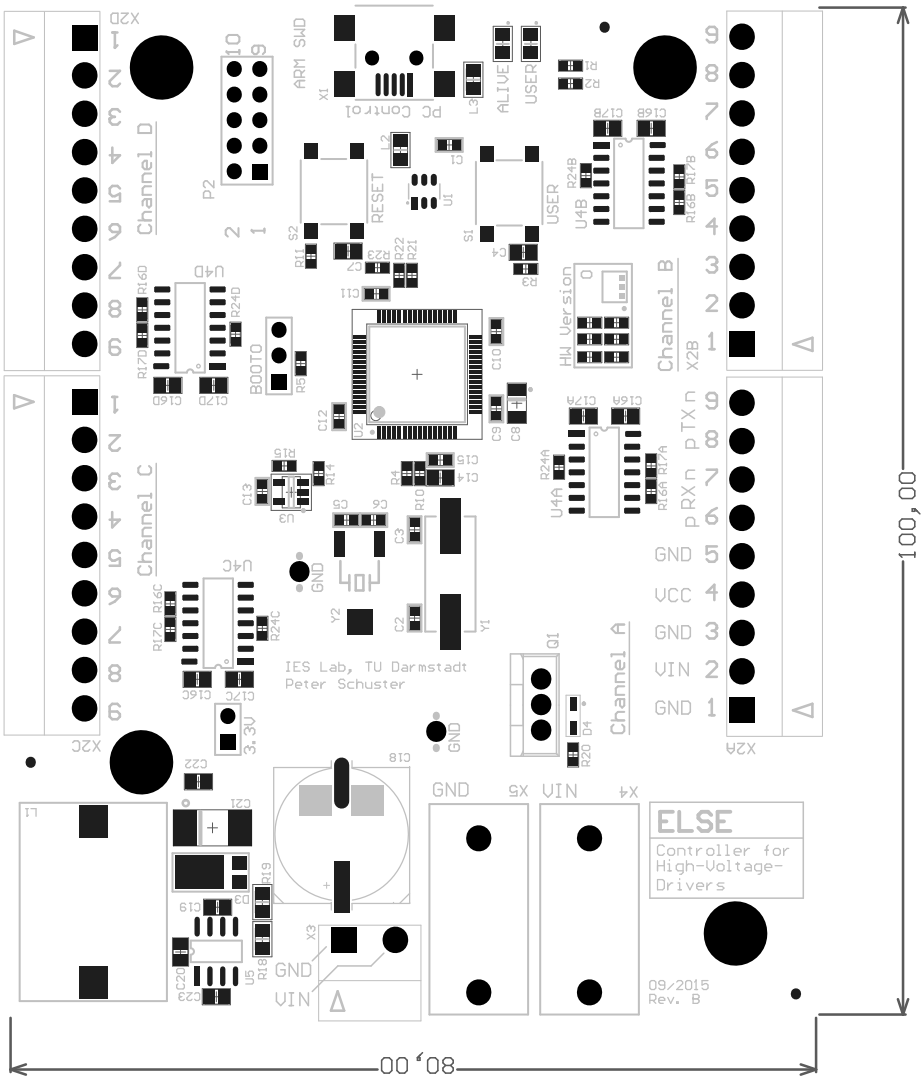
B.3 Assembly Drawings

B.3.1 Driver Board



160,00 (mm)
100,00 (mm)
IES Lab, TU Darmstadt
Peter Schuster 09/2015, Rev. B
Vout
GND
Vout
GND
High Voltage
High Voltage
C1
C2
C3
C4
C5
C6
C8

B.3.2 Controller Board



B.4 Bill of Materials

B.4.1 Driver Board

Desig.	Value	Description	Manufacturer No.
C1	470μF	CAP ALUM 470UF 20% 80V SMD	EEV-FK1K471M
C2	150μF	CAP ALUM 150UF 20% 80V SMD	EEV-FK1K151Q
C3	22μF	CAP ALUM 22UF 20% 250V RADIAL	EEU-EE2E220
C4	22μF	CAP ALUM 22UF 20% 250V RADIAL	EEU-EE2E220
C5	220μF	CAP ALUM 220UF 20% 250V RADIAL	B43821F2227M
C6	220μF	CAP ALUM 220UF 20% 250V RADIAL	B43821F2227M
C13	1μF	CAP CER 1UF 100V 10% X7S 0805	C2012X7S2A105K125AB
C14	1μF	CAP CER 1UF 50V 10% X7R 0805	CL21B105KBFNNNE
C15	220pF	CAP CER 220PF 50V 5% NP0 0805	CL21C221JBANNNC
C16	10nF	CAP CER 10000PF 25V 10% X7R 0805	C0805C103K3RACTU
C17	3300pF	CAP CER 3300PF 50V 5% C0G 0805	C2012C0G1H332J060AA

C18	1000pF	CAP CER 1000PF 25V 10% X7R 0603	C0603C102K3RACTU
C19	1μF	CAP CER 1UF 50V 10% X7R 0805	CL21B105KBFNNNE
C20	10000pF	CAP CER 10000PF 100V X7R 0805	C0805C103K1RACTU
C21	22μF	CAP ALUM 22UF 20% 16V SMD	EEE-FK1C220UR
C22	4700pF	CAP CER 4700PF 25V 5% C0G 0603	C1608C0G1E472J080AA
C23	22μF	CAP ALUM 22UF 20% 16V SMD	EEE-FK1C220UR
C24	22μF	CAP ALUM 22UF 20% 16V SMD	EEE-FK1C220UR
C33	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C34	15pF	CAP CER 15PF 50V 1% NP0 0603	CL10C150FB8NNWC
C35	15pF	CAP CER 15PF 50V 1% NP0 0603	CL10C150FB8NNWC
C36	27pF	CAP CER 27PF 50V 1% NP0 0603	CL10C270FB8NNNC
C37	27pF	CAP CER 27PF 50V 1% NP0 0603	CL10C270FB8NNNC
C38	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C39	10μF	CAP TANT 10UF 16V 10% 1206	T491A106K016AT
C40	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C41	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C42	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C43	1μF	CAP CER 1UF 50V 10% X7R 0805	CL21B105KBFNNNE
C44	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C45	10μF	CAP TANT 10UF 16V 10% 1206	T491A106K016AT
C46	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C47	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C48	1μF	CAP CER 1UF 50V 10% X7R 0805	CL21B105KBFNNNE
C49	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C50	100pF	CAP CER 100PF 50V 5% C0G 0603	C1608C0G1H101J080AA
C52	100pF	CAP CER 100PF 50V 5% C0G 0603	C1608C0G1H101J080AA
C53	10pF	CAP CER 10PF 250V 5% NP0 0805	GRM21A5C2E100JW01D
C54	1μF	CAP CER 1UF 50V 10% X7R 0805	CL21B105KBFNNNE
C55	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C56	1μF	CAP CER 1UF 50V 10% X7R 0805	CL21B105KBFNNNE
C57	10μF	CAP TANT 10UF 35V 10% 2413	T491C106K035AT
C58	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C59	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C60	7pF	CAP CER 7PF 250V NP0 0805	CBR08C709CAGAC
C61	10000pF	CAP CER 10000PF 250V 5% X7R 1206	C1206C103JARACTU
C62	0.1μF	CAP CER 0.1UF 250V 10% X7R 1206	C3216X7R2E104K160AA
C63	10000pF	CAP CER 10000PF 250V 5% X7R 1206	C1206C103JARACTU
C64	10μF	CAP TANT 10UF 16V 10% 1206	T491A106K016AT
C65	10000pF	CAP CER 10000PF 100V X7R 0805	C0805C103K1RACTU
C66	1000pF	CAP CER 1000PF 100V 10% X7R 0603	C1608X7R2A102K080AA
C67	1μF	CAP CER 1UF 100V 10% X7S 0805	C2012X7S2A105K125AB
C68	10μF	CAP ALUM 10UF 20% 80V SMD	EEE-FK1K100P
C69	0.1μF	CAP CER 0.1UF 250V 10% X7R 1206	C3216X7R2E104K160AA
C70	10μF	CAP ALUM 10UF 20% 80V SMD	EEE-FK1K100P
C71	1μF	CAP CER 1UF 100V 10% X7S 0805	C2012X7S2A105K125AB
C72	1μF	CAP CER 1UF 100V 10% X7S 0805	C2012X7S2A105K125AB
C73	2.2μF	CAP CER 2.2UF 35V 10% X7R 0805	C2012X7R1V225K085AC

C74	2.2μF	CAP CER 2.2UF 35V 10% X7R 0805	C2012X7R1V225K085AC
C75	2.2μF	CAP CER 2.2UF 35V 10% X7R 0805	C2012X7R1V225K085AC
D1	-	Surface Mount Ultrafast Power Rectifier, 2-Pin SMA	MURA130T3G
D2	-	Surface Mount Ultrafast Power Rectifier, 2-Pin SMA	MURA130T3G
D3	-	Surface Mount Ultrafast Power Rectifier, 2-Pin SMA	MURA130T3G
D4	-	Schottky Power Rectifier, Surface Mount Power Package, 2-Pin SMB	MBRS190T3G
D5	-	Schottky Power Rectifier, Surface Mount Power Package, 2-Pin SMB	MBRS190T3G
D6	-	Schottky Power Rectifier, Surface Mount Power Package, 2-Pin SMB	MBRS190T3G
D7	-	Schottky Power Rectifier, Surface Mount Power Package, 2-Pin SMB	MBRS190T3G
D8	-	Schottky Power Rectifier, Surface Mount Power Package, 2-Pin SMB	MBRS190T3G
D9	-	Schottky Power Rectifier, Surface Mount Power Package, 2-Pin SMB	MBRS190T3G
D11	-	Zener Voltage Regulator, 300 mW, Tight Tolerance Portfolio, 2-Pin SOD-323	MM3Z3V3ST1G
D12	-	LED GREEN CLEAR 0805 SMD	LTST-C170GKT
D13	-	LED GREEN CLEAR 0805 SMD	LTST-C170GKT
D14	-	LED GREEN CLEAR 0805 SMD	LTST-C170GKT
D15	-	LED GREEN CLEAR 0805 SMD	LTST-C170GKT
D16	-	LED GREEN CLEAR 0805 SMD	LTST-C170GKT
D17	1N4148	DIODE GEN PURP 100V 200MA SOD80	LL4148
D18	1N4148	DIODE GEN PURP 100V 200MA SOD80	LL4148
D19	1N4148	DIODE GEN PURP 100V 200MA SOD80	LL4148
D20	1N4148	DIODE GEN PURP 100V 200MA SOD80	LL4148
L1	-	FERRITE CHIP 600 OHM 0805	BLM21RK601SN1D
L2	-	FERRITE CHIP 600 OHM 0805	BLM21RK601SN1D
L3	-	FERRITE CHIP 600 OHM 0805	BLM21RK601SN1D
L4	-	FERRITE CHIP 600 OHM 0805	BLM21RK601SN1D
P1	-	Header, 3-Pin	
P2	-	Header, 5-Pin, Dual row	SBH11-PBPC-D05-ST-BK
P3	-	Header, 2-Pin	
P4	-	Header, 2-Pin	
P5	-	Header, 2-Pin	
P6	-	Header, 2-Pin	
P7	-	Header, 2-Pin	
P8	-	Header, 3-Pin	
P9	-	Header, 3-Pin	
Q1	-	MOSFET N-CH 250V 60A TO-220AB	IRFB4332PBF
Q2	-	TRANS NPN 500V 0.5A SOT-23	STR1550
Q3	-	TRANS PNP 500V 0.5A SOT-23	STR2550
Q4	-	TRANS PNP 500V 0.5A SOT-23	STR2550

Q5	-	TRANS NPN 500V 0.5A SOT-23	STR1550
Q6	-	TRANS PNP 500V 0.5A SOT-23	STR2550
Q7	-	TRANS PNP 500V 0.5A SOT-23	STR2550
Q8	-	TRANS NPN 500V 0.5A SOT-23	STR1550
Q9	-	TRANS PNP 500V 0.5A SOT-23	STR2550
Q10	-	TRANS PNP 500V 0.5A SOT-23	STR2550
Q11	-	TRANS PNP 500V 0.5A SOT-23	STR2550
Q12	-	TRANS NPN 500V 0.5A SOT-23	STR1550
Q13	-	TRANS PNP 500V 0.5A SOT-23	STR2550
R1	20K	RES SMD 20K OHM 1% 1/8W 0805	MCR10ERTF2002
R2	12	RES SMD 12 OHM 5% 1W 2512	MCR100JZHJ120
R3	402K	RES SMD 402K OHM 1% 1/4W 1206	KTR18EZPF4023
R4	15K	RES SMD 15K OHM 1% 1/8W 0805	MCR10ERTF1502
R5	20K	RES SMD 20K OHM 1% 1/10W 0603	MCR03ERTF2002
R6	2.4k	RES SMD 2.4K OHM 1% 1/8W 0805	KTR10EZPF2401
R7	0.047	RES SMD 0.047 OHM 1% 1/2W 1206	UCR18EVHFSR047
R8	340K	RES SMD 340K OHM 1% 1/10W 0603	MCR03ERTF3403
R9	20K	RES SMD 20K OHM 1% 1/8W 0805	MCR10ERTF2002
R10	105K	RES SMD 105K OHM 1% 1/8W 0805	MCR10ERTF1053
R11	180	RES SMD 180 OHM 1% 1/10W 0603	MCR03ERTF1800
R12	180	RES SMD 180 OHM 1% 1/10W 0603	MCR03ERTF1800
R13	180	RES SMD 180 OHM 1% 1/10W 0603	MCR03ERTF1800
R14	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R15	4.7k	RES SMD 4.7K OHM 1% 1/10W 0603	MCR03ERTF4701
R16	1K	RES SMD 1K OHM 1% 1/10W 0603	MCR03ERTF1001
R17	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R18	150	RES SMD 150 OHM 1% 1/10W 0603	MCR03ERTF1500
R19	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R22	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R24	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R25	4.7k	RES SMD 4.7K OHM 1% 1/10W 0603	MCR03ERTF4701
R26	4.7k	RES SMD 4.7K OHM 1% 1/10W 0603	MCR03ERTF4701
R27	330	RES SMD 330 OHM 1% 1/8W 0805	MCR10ERTF3300
R28	330	RES SMD 330 OHM 1% 1/8W 0805	MCR10ERTF3300
R29	0.1	RES SMD 0.1 OHM 1% 1/2W 1206	UCR18EVHFLR100
R30	180k	RES SMD 180K OHM 1% 1/8W 0805	KTR10EZPF1803
R31	180k	RES SMD 180K OHM 1% 1/8W 0805	KTR10EZPF1803
R32	300K	RES SMD 300K OHM 1% 1/10W 0603	MCR03ERTF3003
R33	22K	RES SMD 22K OHM 1% 1/10W 0603	MCR03ERTF2202
R34	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R35	20k	TRIMMER 20K OHM 0.5W SMD	3361P-1-203GLF
R36	40.2K	RES SMD 40.2K OHM 1% 1/8W 0805	MCR10ERTF4022
R37	20K	RES SMD 20K OHM 1% 1/8W 0805	MCR10ERTF2002
R38	330	RES SMD 330 OHM 1% 1/8W 0805	MCR10ERTF3300
R39	1K	RES SMD 1K OHM 1% 1/4W 1206	KTR18EZPF1001
R40	20K	RES SMD 20K OHM 1% 1/8W 0805	MCR10ERTF2002
R41	301K	RES SMD 301K OHM 1% 1/4W 1206	MCR18ERTF3013

R42	301K	RES SMD 301K OHM 1% 1/4W 1206	MCR18ERTF3013
R43	100	RES SMD 100 OHM 1% 2W 2512	CRM2512-FX-1000ELF
R44	100	RES SMD 100 OHM 1% 2W 2512	CRM2512-FX-1000ELF
R45	20K	RES SMD 20K OHM 1% 1/8W 0805	MCR10ERTF2002
R46	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R47	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R48	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R49	20	RES SMD 20 OHM 1% 1/4W 1206	MCR18ERTF20R0
R50	1K	RES SMD 1K OHM 1% 1/4W 1206	KTR18EZPF1001
R51	560K	RES SMD 560K OHM 1% 1/8W 0805	MCR10ERTF5603
R52	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R53	100k	RES SMD 100K OHM 1% 1/8W 0805	KTR10EZPF1003
R54	102K	RES SMD 102K OHM 1% 1/8W 0805	KTR10EZPF1023
R55	102K	RES SMD 102K OHM 1% 1/8W 0805	KTR10EZPF1023
R56	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R57	1K	RES SMD 1K OHM 1% 1/4W 1206	MCR18ERTF1001
R58	180K	RES SMD 180K OHM 1% 1/4W 1206	KTR18EZPF1803
R59	2K	RES SMD 2K OHM 1% 1/4W 1206	MCR18ERTF2001
R60	2K	RES SMD 2K OHM 1% 1/4W 1206	MCR18ERTF2001
R61	20K	RES SMD 20K OHM 1% 1/8W 0805	MCR10ERTF2002
R62	180K	RES SMD 180K OHM 1% 1/4W 1206	KTR18EZPF1803
R63	330	RES SMD 330 OHM 1% 1/8W 0805	MCR10ERTF3300
R64	100	RES SMD 100 OHM 1% 1/10W 0603	MCR03ERTF1000
R66	1	RES SMD 1 OHM 1% 1/8W 0805	KTR10EZPF1R00
R67	1	RES SMD 1 OHM 1% 1/8W 0805	KTR10EZPF1R00
R68	1	RES SMD 1 OHM 1% 1/8W 0805	KTR10EZPF1R00
R69	1	RES SMD 1 OHM 1% 1/8W 0805	KTR10EZPF1R00
R70	1	RES SMD 1 OHM 1% 1/8W 0805	KTR10EZPF1R00
R71	1	RES SMD 1 OHM 1% 1/8W 0805	KTR10EZPF1R00
R72	120	RES SMD 120 OHM 1% 1/10W 0603	MCR03ERTF1200
R73	120	RES SMD 120 OHM 1% 1/10W 0603	MCR03ERTF1200
R74	20K	RES SMD 20K OHM 1% 1/8W 0805	MCR10ERTF2002
R75	21K	RES SMD 21K OHM 1% 1/10W 0603	MCR03ERTF2102
R76	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R77	100	RES SMD 100 OHM 1% 1/10W 0603	MCR03ERTF1000
S1	-	SWITCH TACTILE SPST-NO 0.05A 12V	PTS645SL50SMTR92 LFS
S2	-	SWITCH TACTILE SPST-NO 0.05A 12V	PTS645SL50SMTR92 LFS
T1	-	Flyback Transformer	750311889
T2	-	TRANS FLYBACK LM5017 WE-FB	750313995
TP1	-	TERM PC TEST POINT LOOP .445L"	4952
TP2	-	TERM PC TEST POINT LOOP .445L"	4952
TP3	-	TERM PC TEST POINT LOOP .445L"	4952
TP4	-	TERM PC TEST POINT LOOP .445L"	4952
TP5	-	PC TEST POINT MINI SMD	5017
TP6	-	TERM PC TEST POINT LOOP .445L"	4952
TP7	-	TERM PC TEST POINT LOOP .445L"	4952
TP9	-	TERM PC TEST POINT LOOP .445L"	4952

TP10	-	PC TEST POINT MINI SMD	5017
U1	-	IC REG CTRLR PWM CM 10-MSOP	LM5020MM-1/NOPB
U2	-	IC REG BUCK ADJ 0.6A SYNC 8SOPWR	LM5017MR/NOPB
U3	-	ARM Cortex-M0 MCU with 128 Kbytes Flash, 48 MHz CPU, USB	STM32F072CBT6
U4	-	16Kbit, 400kHz, 2.5V, I2C Serial EEPROM, 5-Pin SOT-23	24LC16BT-E/OT
U5	-	TXRX RS-485 0.5MBPS FULL 14SOIC	MAX13432EESD+
U6	-	60V Common Mode, 100 x Gain, Bidirectional Precision Current Sensing Amplifier	LMP8603QMA/NOPB
U7	-	Dual Channel, Precision Operational Amplifier, 20 MHz Typical GBW, 6 V/us SR, 3 to 36 V	LT1678CS8#PBF
U8	-	IC DGTL POT 1024POS 20K 14TSSOP	AD5293BRUZ-20-RL7
X1	-	Phoenix Contact Mini Combicon	1803345
X2	-	Phoenix Contact Mini Combicon	1803345
X3	-	Phoenix Contact MKDSN 1,5/ 2-5,08	1729128
X4	-	Phoenix Contact Mini Combicon	1836189
Y1	-	Crystal Oscillator 32.768 kHz	CMR200T32768DZFT
Y2	-	Crystal Oscillator 8 MHz	9C-8.000MBBK-T

B.4.2 Controller Board

Desig.	**Value**	**Description**	**Manufacturer No.**
C1	0.1μF	CAP CER 0.1UF 50V 10% X7R 0603	CL10B104KB8SFNC
C2	27pF	CAP CER 27PF 50V 1% NP0 0603	CL10C270FB8NNNC
C3	27pF	CAP CER 27PF 50V 1% NP0 0603	CL10C270FB8NNNC
C4	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C5	15pF	CAP CER 15PF 50V 1% NP0 0603	CL10C150FB8NNWC
C6	15pF	CAP CER 15PF 50V 1% NP0 0603	CL10C150FB8NNWC
C7	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C8	10μF	CAP TANT 10UF 16V 10% 1206	T491A106K016AT
C9	0.1μF	CAP CER 0.1UF 50V 10% X7R 0603	CL10B104KB8SFNC
C10	0.1μF	CAP CER 0.1UF 50V 10% X7R 0603	CL10B104KB8SFNC
C11	0.1μF	CAP CER 0.1UF 50V 10% X7R 0603	CL10B104KB8SFNC
C12	0.1μF	CAP CER 0.1UF 50V 10% X7R 0603	CL10B104KB8SFNC
C13	0.1μF	CAP CER 0.1UF 50V 10% X7R 0603	CL10B104KB8SFNC
C14	1μF	CAP CER 1UF 50V 10% X7R 0805	CL21B105KBFNNNE
C15	0.1μF	CAP CER 0.1UF 50V 10% X7R 0603	CL10B104KB8SFNC
C16A	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C16B	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C16C	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C16D	0.1μF	CAP CER 0.1UF 50V 10% X7R 0805	CL21B104KBCNNNC
C17A	1μF	CAP CER 1UF 50V 10% X7R 0805	CL21B105KBFNNNE
C17B	1μF	CAP CER 1UF 50V 10% X7R 0805	CL21B105KBFNNNE
C17C	1μF	CAP CER 1UF 50V 10% X7R 0805	CL21B105KBFNNNE
C17D	1μF	CAP CER 1UF 50V 10% X7R 0805	CL21B105KBFNNNE
C18	68μF	CAP ALUM 68UF 20% 100V SMD	EEV-FK2A680Q

C19	1μF	CAP CER 1UF 100V 10% X7S 0805	C2012X7S2A105K125AB
C20	0.1μF	CAP CER 0.1UF 100V 10% X7R 0805	CL21B104KCC5PNC
C21	68 uF	Tantalum Capacitors - Solid SMD 68uF 16volts 10% C case Conformal	594D686X9010C2T
C22	2.2μF	CAP CER 2.2UF 35V 10% X7R 0805	C2012X7R1V225K085AC
C23	0.1μF	CAP CER 0.1UF 100V 10% X7R 0805	CL21B104KCC5PNC
D1	-	LED GREEN CLEAR 0805 SMD	LTST-C170GKT
D2	-	LED GREEN CLEAR 0805 SMD	LTST-C170GKT
D3	-	DIODE SCHOTTKY 100V 5A POWERDI5	PDS5100-13
D4	-	DIODE ZENER 12V 200MW SOD323	BZT52C12S-7-F
L1	-	Fixed Inductors DO5022P Pwr Inductor 100 uH 20 % 1.8 A	DO5022P-104MLB
L2	-	FERRITE CHIP 600 OHM 0805	BLM21RK601SN1D
L3	-	FERRITE CHIP 600 OHM 0805	BLM21RK601SN1D
P1	-	Header, 3-Pin	
P2	-	Header, 5-Pin, Dual row	SBH11-PBPC-D05-ST-BK
P3	-	Header, 2-Pin	
Q1	-	MOSFET P-CH 100V 23A TO-220AB	IRF9540NPBF
R1	180	RES SMD 180 OHM 1% 1/10W 0603	MCR03ERTF1800
R2	180	RES SMD 180 OHM 1% 1/10W 0603	MCR03ERTF1800
R3	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R4	150	RES SMD 150 OHM 1% 1/10W 0603	MCR03ERTF1500
R5	4.7k	RES SMD 4.7K OHM 1% 1/10W 0603	MCR03ERTF4701
R7	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R9	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R10	1K	RES SMD 1K OHM 1% 1/10W 0603	MCR03ERTF1001
R11	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R13	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R14	4.7k	RES SMD 4.7K OHM 1% 1/10W 0603	MCR03ERTF4701
R15	4.7k	RES SMD 4.7K OHM 1% 1/10W 0603	MCR03ERTF4701
R16A	120	RES SMD 120 OHM 1% 1/10W 0603	MCR03ERTF1200
R16B	120	RES SMD 120 OHM 1% 1/10W 0603	MCR03ERTF1200
R16C	120	RES SMD 120 OHM 1% 1/10W 0603	MCR03ERTF1200
R16D	120	RES SMD 120 OHM 1% 1/10W 0603	MCR03ERTF1200
R17A	120	RES SMD 120 OHM 1% 1/10W 0603	MCR03ERTF1200
R17B	120	RES SMD 120 OHM 1% 1/10W 0603	MCR03ERTF1200
R17C	120	RES SMD 120 OHM 1% 1/10W 0603	MCR03ERTF1200
R17D	120	RES SMD 120 OHM 1% 1/10W 0603	MCR03ERTF1200
R18	1000K	RES SMD 1M OHM 1% 1/8W 0805	MCR10ERTF1004
R19	384K	RES SMD 383K OHM 1% 1/8W 0805	MCR10ERTF3833
R20	100K	RES SMD 100K OHM 1% 1/10W 0603	MCR03ERTF1003
R21	15	RES SMD 15 OHM 1% 1/10W 0603	MCR03ERTF15R0
R22	15	RES SMD 15 OHM 1% 1/10W 0603	MCR03ERTF15R0
R23	1.5K	RES SMD 1.5K OHM 1% 1/10W 0603	MCR03ERTF1501
R24A	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R24B	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
R24C	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002

R24D	10K	RES SMD 10K OHM 1% 1/10W 0603	MCR03ERTF1002
S1	-	SWITCH TACTILE SPST-NO 0.05A 12V	PTS645SL50SMTR92 LFS
S2	-	SWITCH TACTILE SPST-NO 0.05A 12V	PTS645SL50SMTR92 LFS
TP1	-	TERM PC TEST POINT LOOP .445L"	4952
TP2	-	TERM PC TEST POINT LOOP .445L"	4952
U1	-	TVS DIODE 5.25VWM 17VC SOT23-6	USBLC6-2SC6
U2	-	ARM Cortex-M3 32-bit MCU, 1024 KB Flash, 96 KB Internal RAM, 51 I/Os, 64-pin LQFP	STM32F103RGT6
U3	-	16Kbit, 400kHz, 2.5V, I2C Serial EEPROM, 5-Pin SOT-23	24LC16BT-E/OT
U4A	-	TXRX RS-485 0.5MBPS FULL 14SOIC	MAX13432EESD+
U4B	-	TXRX RS-485 0.5MBPS FULL 14SOIC	MAX13432EESD+
U4C	-	TXRX RS-485 0.5MBPS FULL 14SOIC	MAX13432EESD+
U4D	-	TXRX RS-485 0.5MBPS FULL 14SOIC	MAX13432EESD+
U5	-	IC REG BUCK 3.3V 1A 8SOIC	MAX5035AASA+
X1	-	CONN USB MINI B R/A SMD	USB-M26FTR
X2A	-	Phoenix Contact Mini Combicon	1803345
X2B	-	Phoenix Contact Mini Combicon	1803345
X2C	-	Phoenix Contact Mini Combicon	1803345
X2D	-	Phoenix Contact Mini Combicon	1803345
X3	-	Phoenix Contact Mini Combicon	1836189
X4	-	DELTRON COMPONENTS - 571-0500-01 - SOCKET, 4MM, LPT, RED	571-0500-01
X5	-	DELTRON COMPONENTS - 571-0100-01 - SOCKET, 4MM PCB BLACK	571-0100-01
Y1	-	Crystal Oscillator 8 MHz	9C-8.000MBBK-T
Y2	-	Crystal Oscillator 32.768 kHz	CMR200T32768DZFT